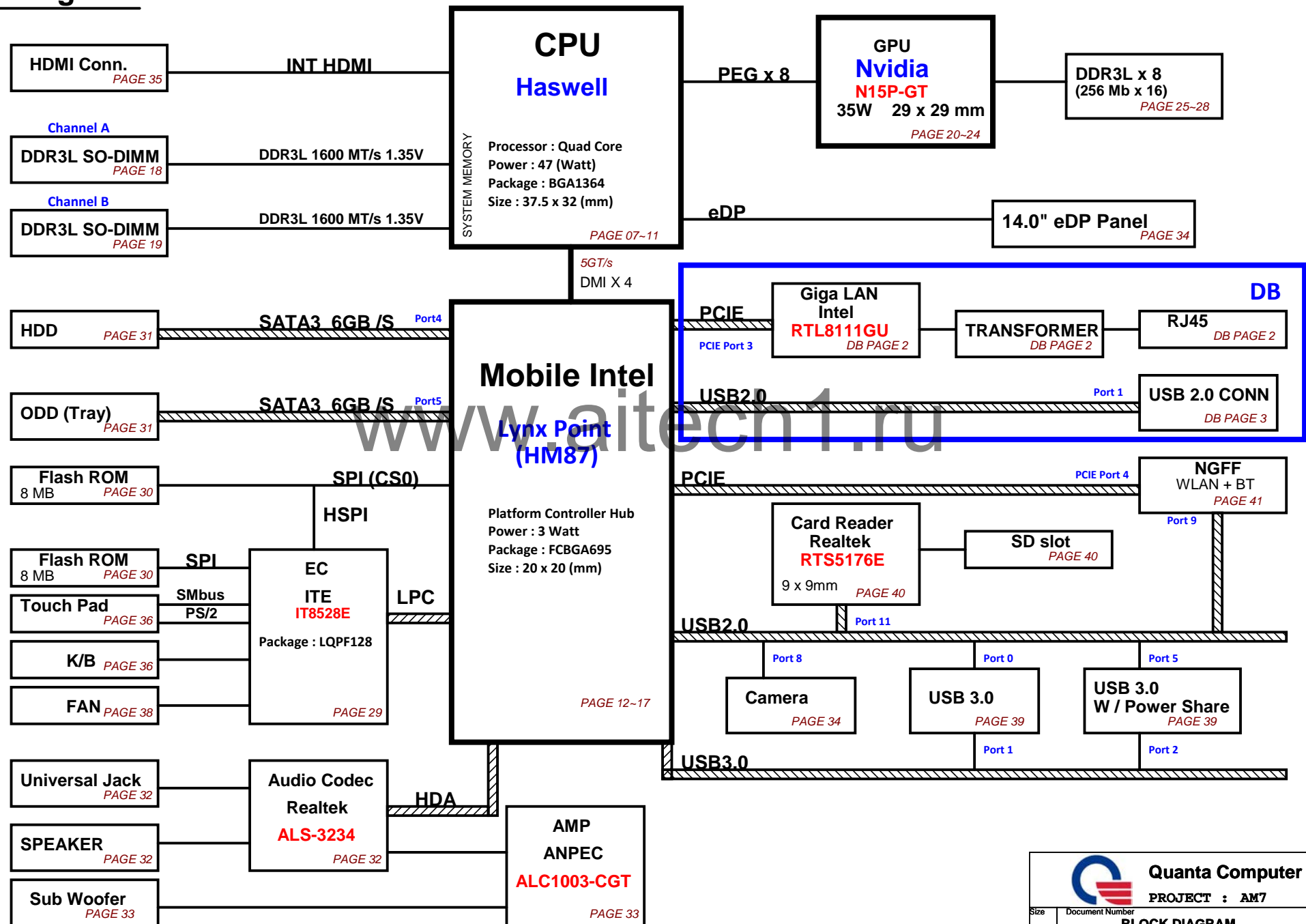
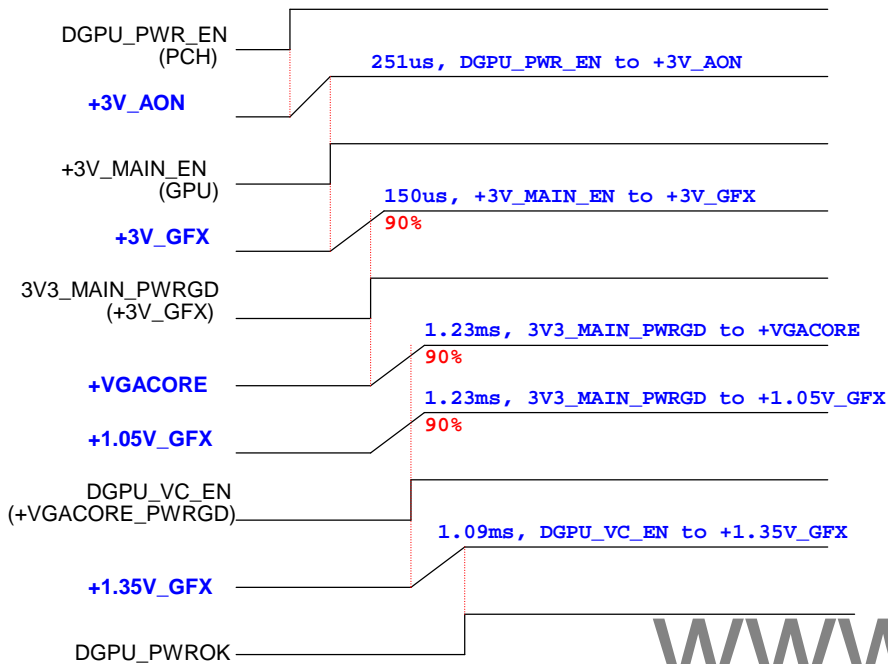


Block Diagram



AM7 GPU Power UP sequence

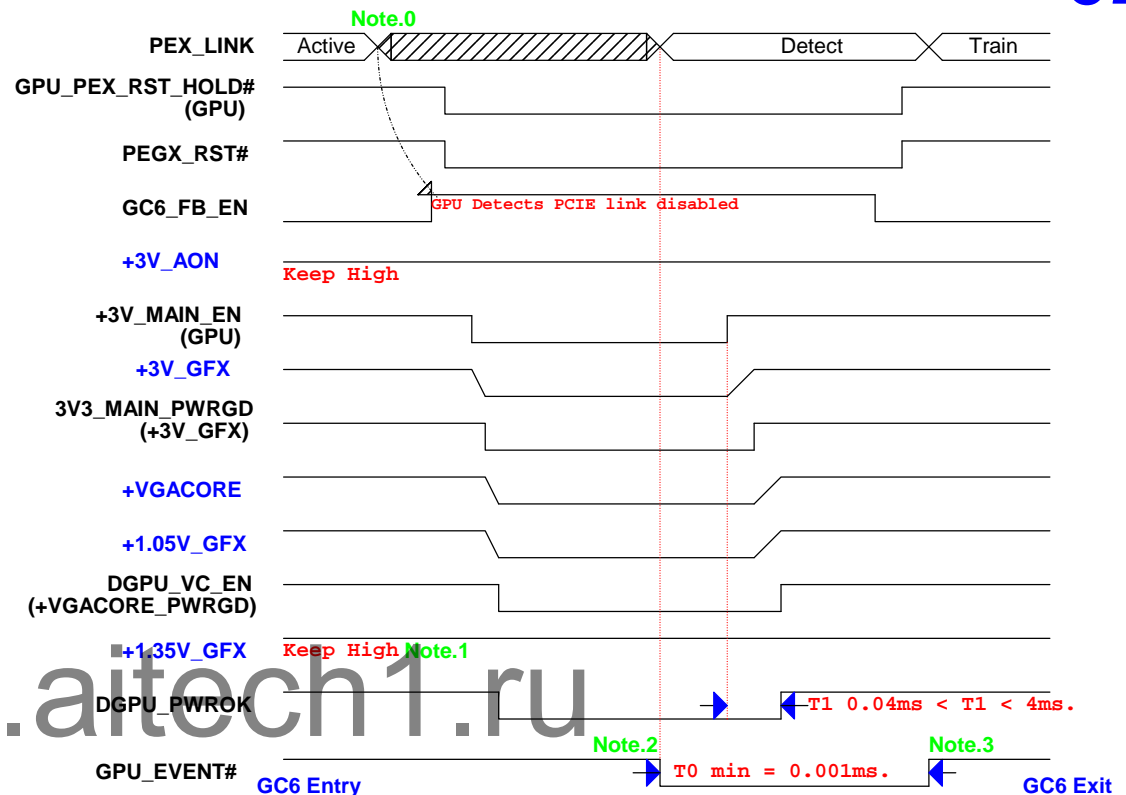


- The ramp time for any rail must be more than 40 μ s and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up

3.10.2.2 Power-Down Sequence

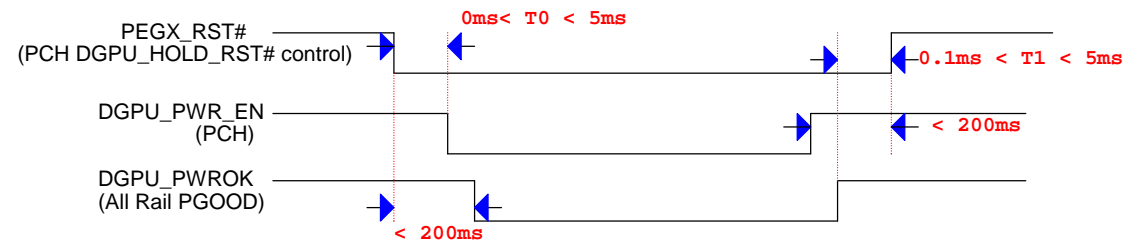
There is no specific power down sequence required. However, residual voltage from power down should not disrupt the power-up sequence when back to back GPU power-down and power-up take place.

AM7 GPU GC62.0 Entry/Exit sequence

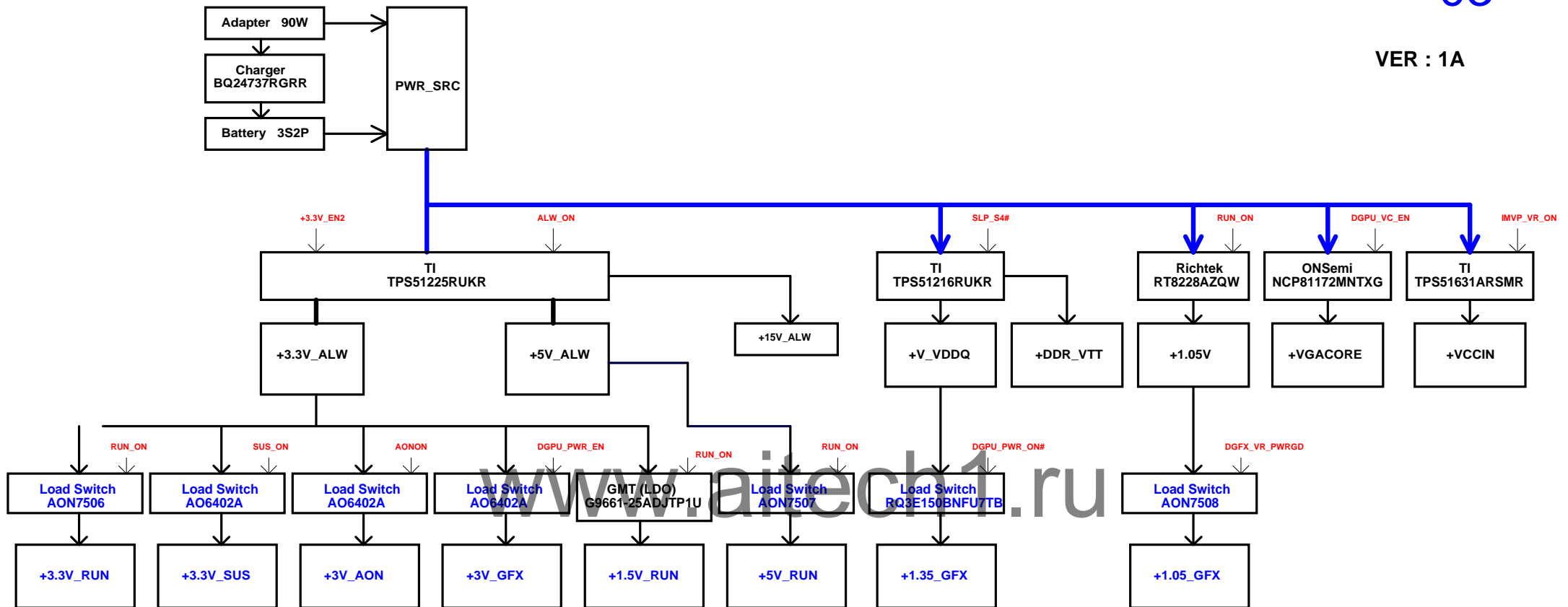


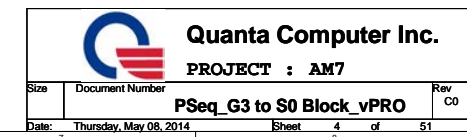
AM7 Optimus GPU On/Off sequence

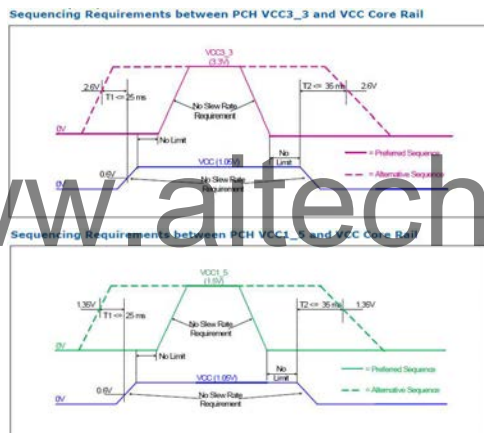
T0 = 220 us, PEGX_RST# to DGPU_PWR_EN
2.21 ms, DGPU_PWR_EN to DGPU_PWROK



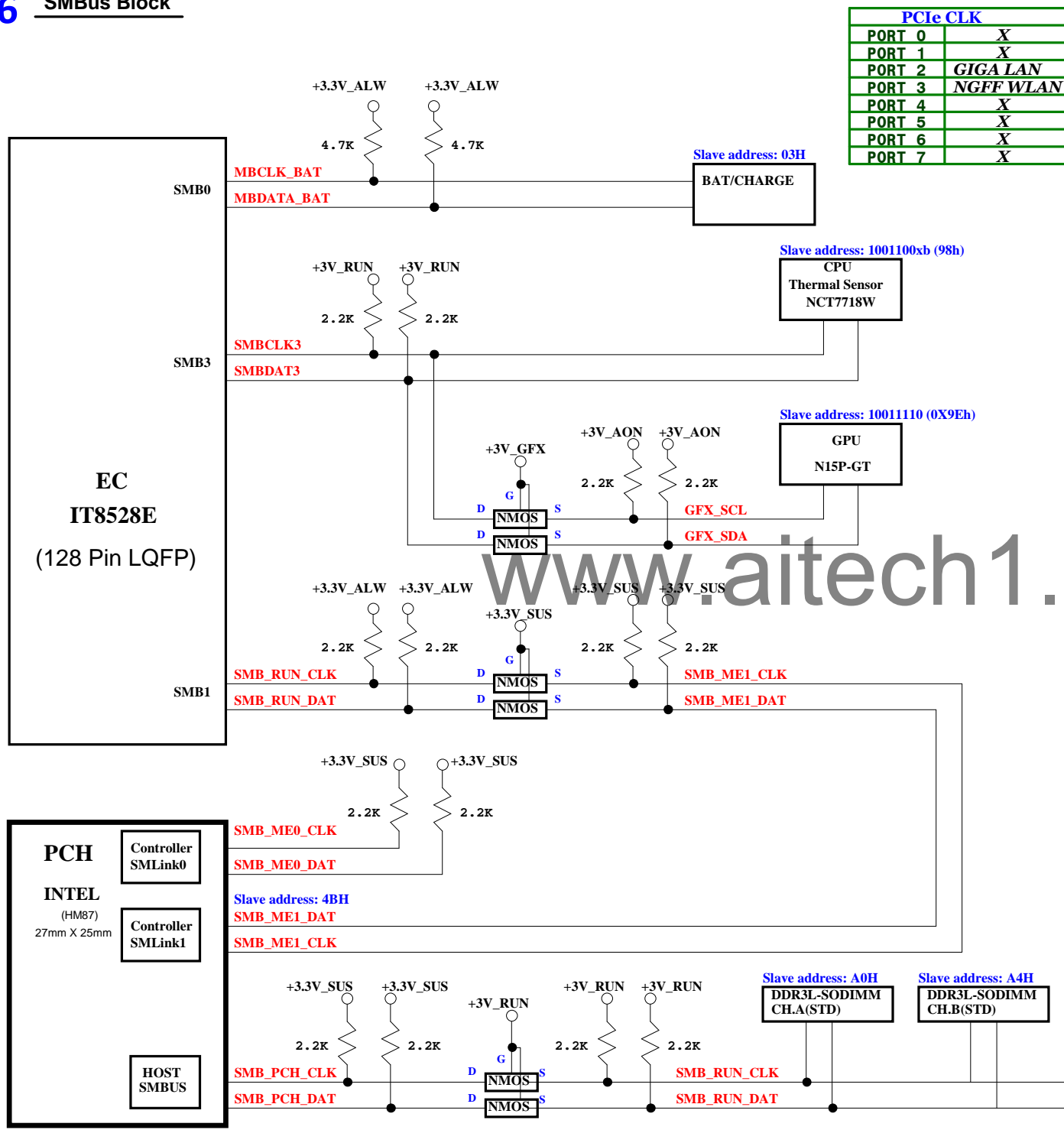
P.S. The entire entry and exit sequence must complete within 200 ms







06 SMBus Block

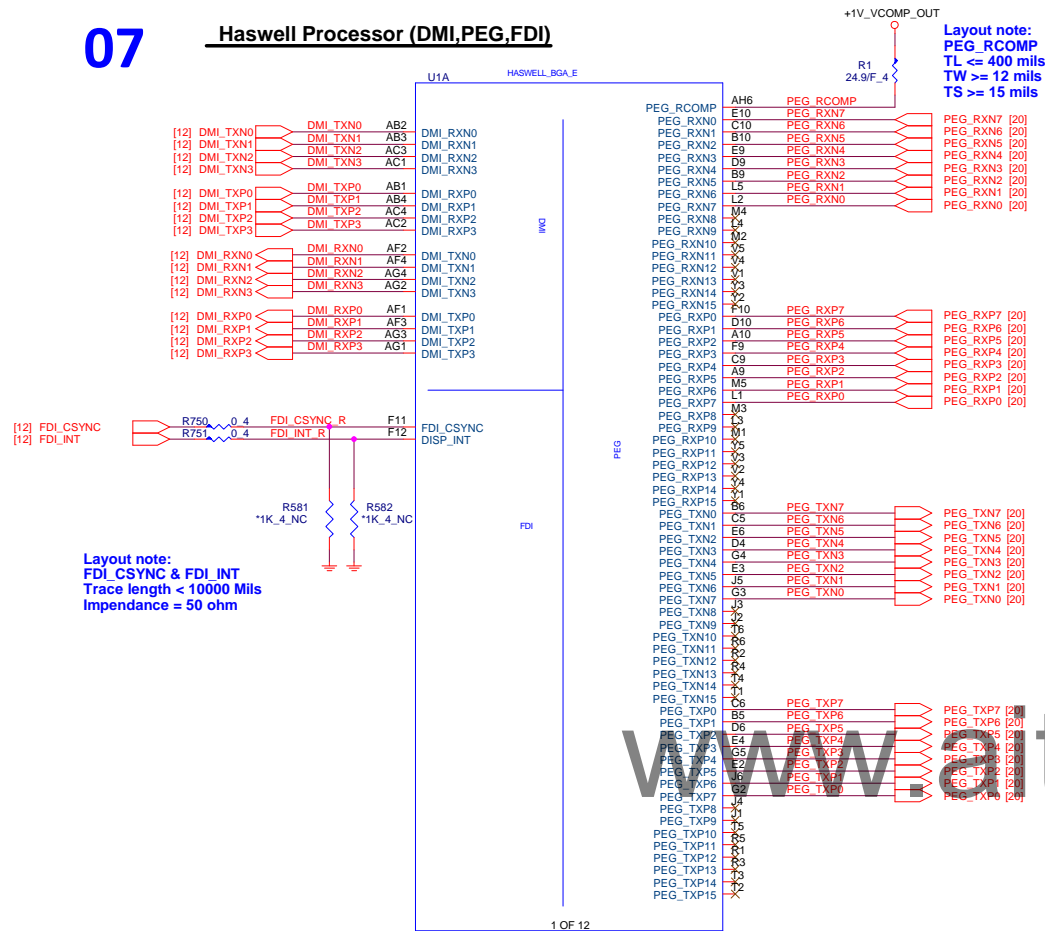


PCIe CLK		
PORT 0		X
PORT 1		X
PORT 2		GIGA LAN
PORT 3		NGFF WLAN
PORT 4		X
PORT 5		X
PORT 6		X
PORT 7		X

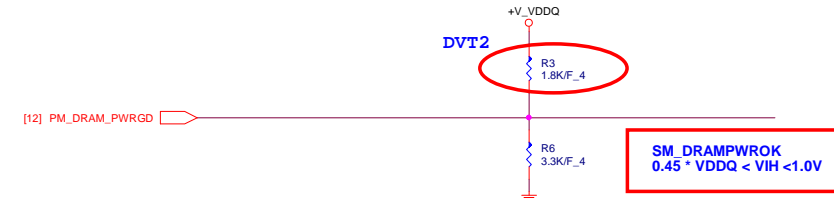
HSIO Port	HM87	AM7
PORT 1	USB3.0 PORT1	USB 3.0 CONN 1
PORT 2	USB3.0 PORT2	USB 3.0 CONN 2
PORT 3	USB3.0 PORT5	X
PORT 4	USB3.0 PORT6	X
PORT 5	USB3.0 PORT3 PCIe* Port 1	X
PORT 6	USB3.0 PORT4 PCIe* Port 2	X
PORT 7	PCIe* Port 3	GIGA LAN
PORT 8	PCIe* Port 4	NGFF WLAN
PORT 9	PCIe* Port 5	X
PORT 10	PCIe* Port 6	X
PORT 11	PCIe* Port 7	X
PORT 12	PCIe* Port 8	X
PORT 13	PCIe* SATA 6Gb/s Port 1 Port 4	SATA HDD
PORT 14	PCIe* SATA 6Gb/s Port 2 Port 5	SATA ODD
PORT 15	SATA 6Gb/s Port 0	X
PORT 16	SATA 6Gb/s Port 1	X
PORT 17	SATA 3Gb/s Port 2	X
PORT 18	SATA 3Gb/s Port 3	X

USB 2.0			
EHCI #1		EHCI #2	
PORT 0	USB3.0 Conn	PORT 8	Camera
PORT 1	USB2.0 CONN / DB	PORT 9	BT
PORT 2	X	PORT 10	X
PORT 3	X	PORT 11	Card reader
PORT 4	X	PORT 12	X
PORT 5	USB3.0 Conn / PS	PORT 13	X
PORT 6	X		
PORT 7	X		

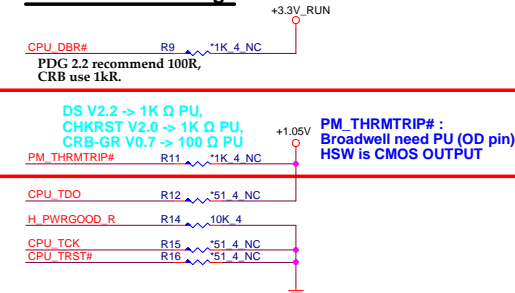
Haswell Processor (DMI,PEG,FDI)



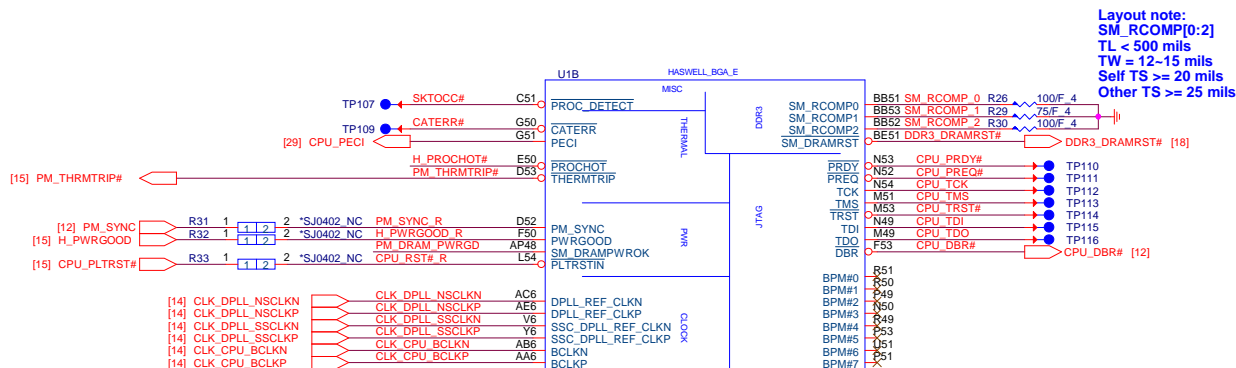
SM_DRAMPWROK# Topology



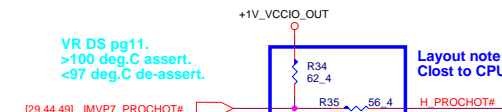
CPU PU/PD setting



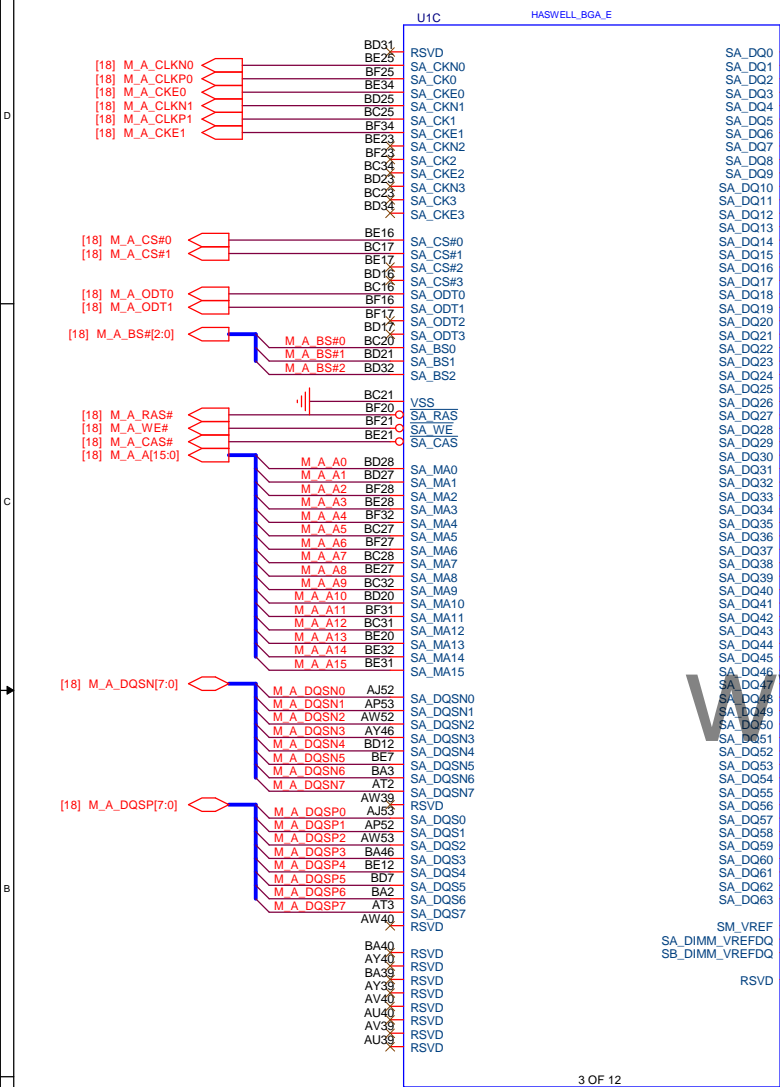
Haswell Processor (CLK,MISC,JTAG)



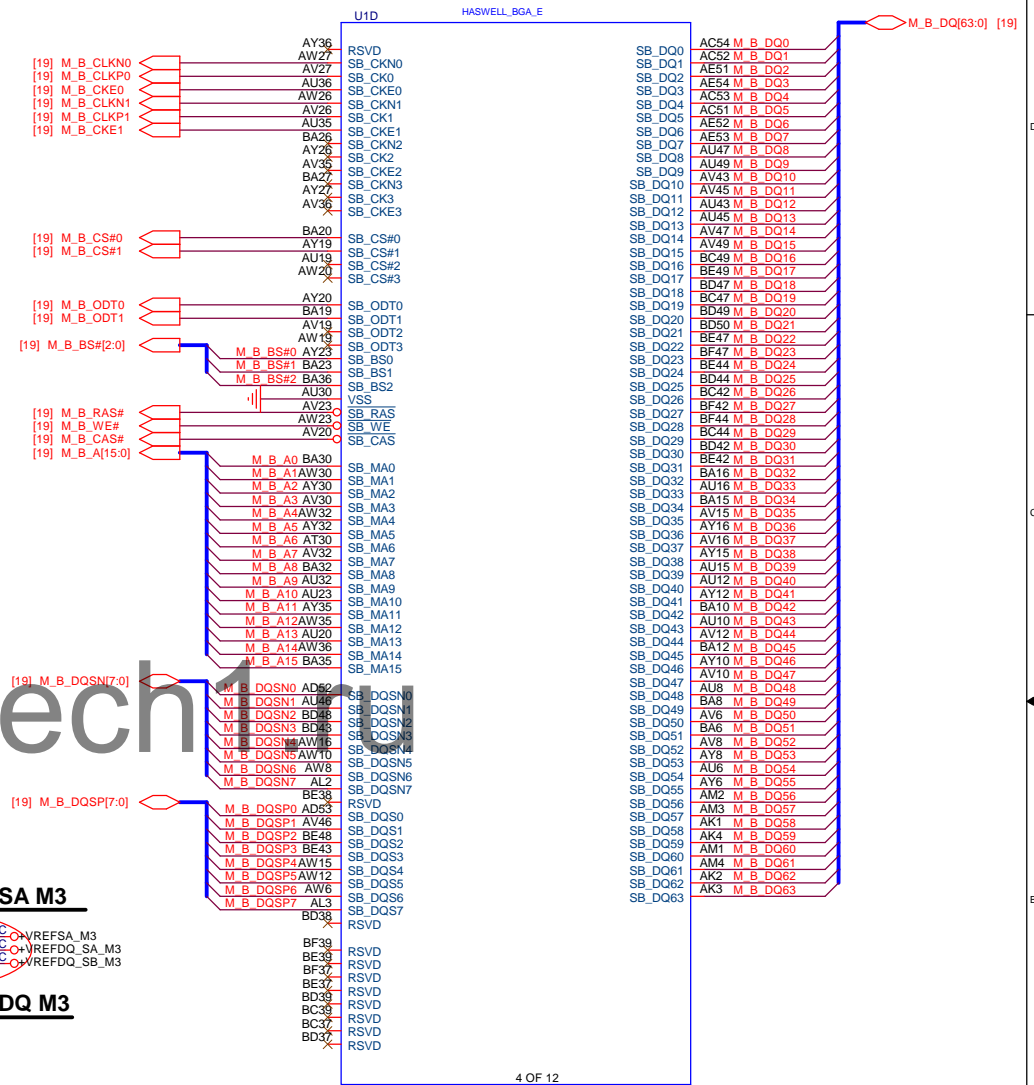
PROCHOT# Topology PDG v2.2



Haswell Processor (DDR3)



Haswell Processor (DDR3)

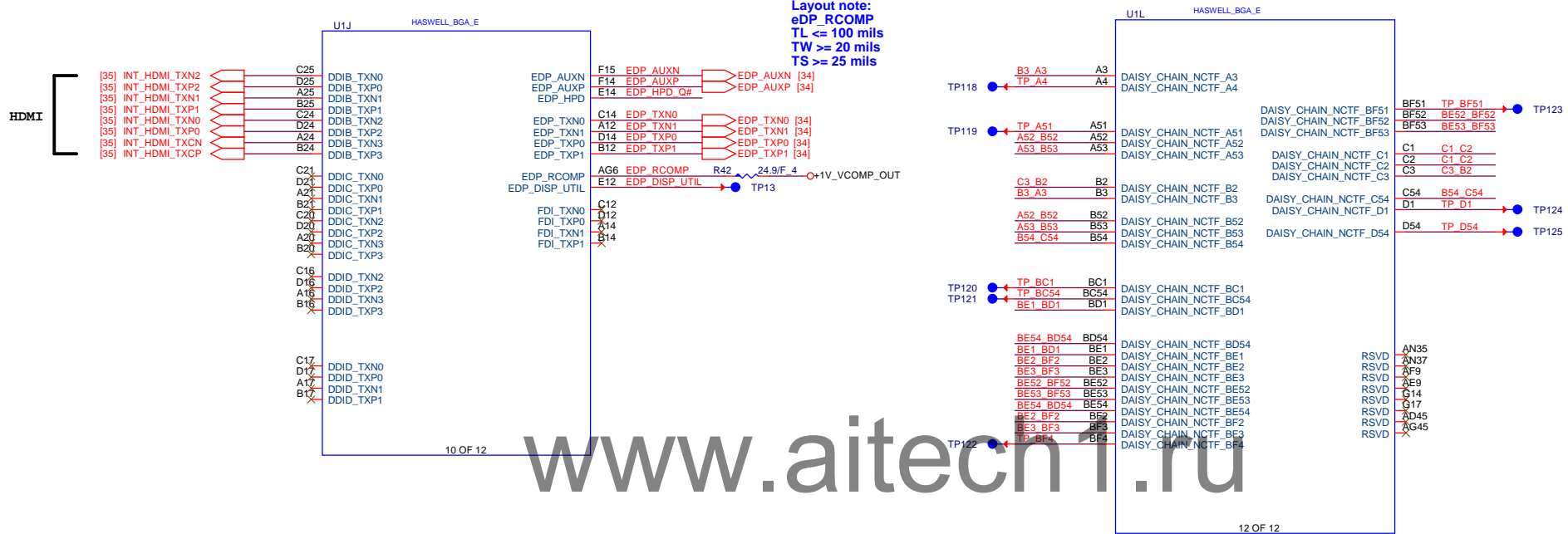
[illegible]

CPU VREFSA M3

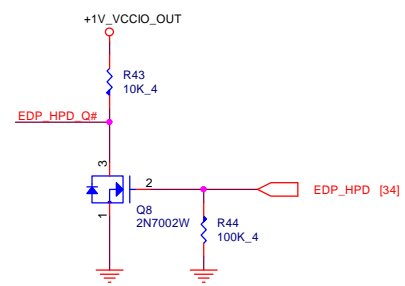
DVT2 CPU VREFDQ M3



Haswell Processor (DDI,eDP,FDI)



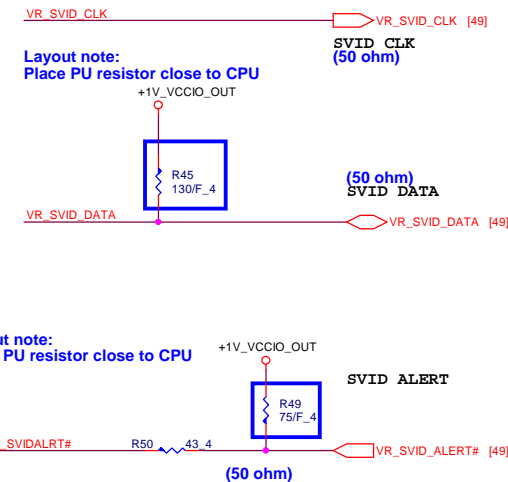
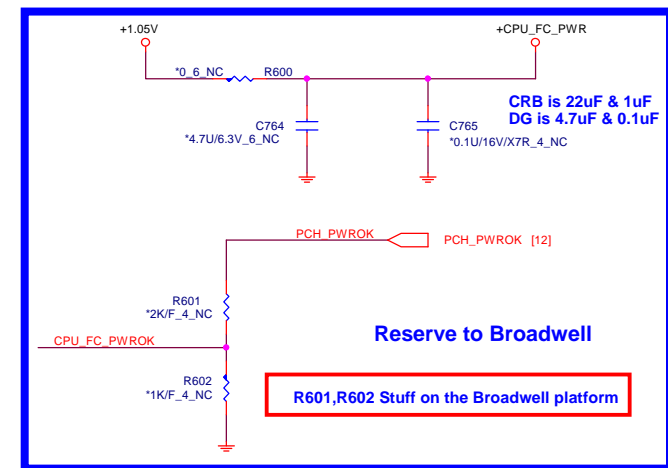
Level Shift



Haswell Processor (POWER)

Layout note:
DC,47W,85ALayout note:
DC,47W,2.1A

SVID

Layout note:
need routing
together and ALERT need
between CLK and DATAOutput capability:
300mAOutput capability:
300mA

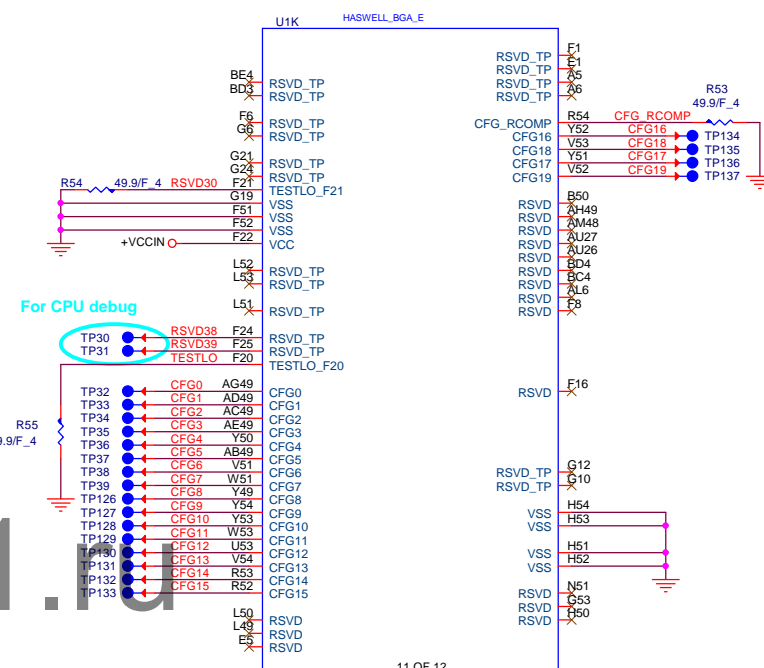
Quanta Computer Inc.

PROJECT : AM7

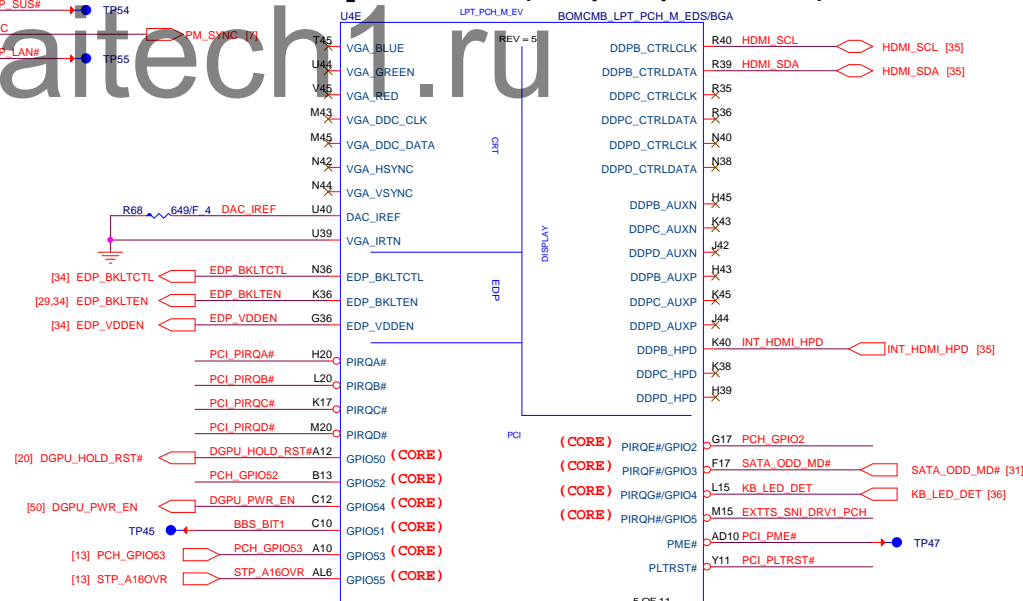
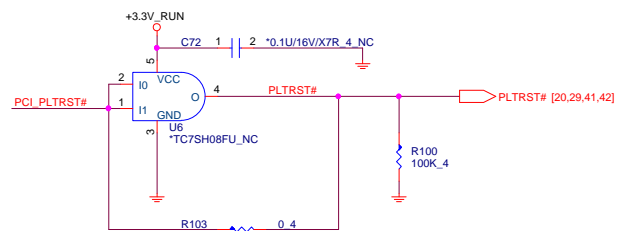
Haswell Processor (GND)

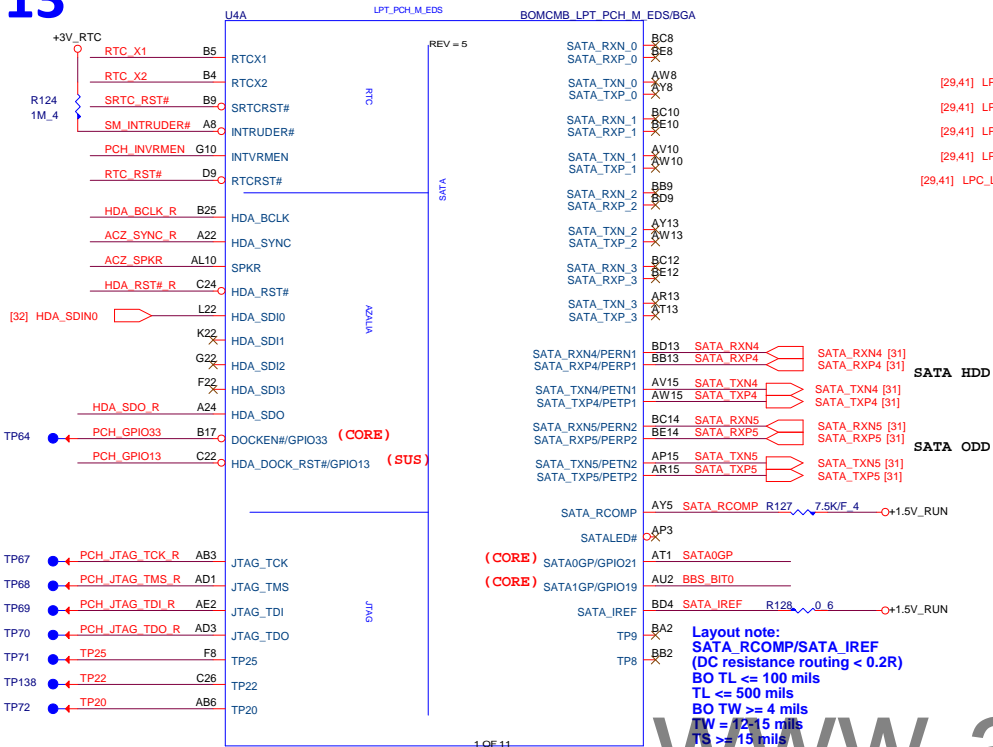


Haswell Processor (CFG,RSVD)

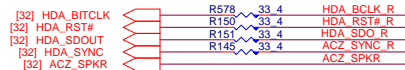


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[3]	MSR Privacy Bit Feature	x1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting x0 = IA32_Debug_Interface_MSR (0xC80) bit[0]. Default setting overridden	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	

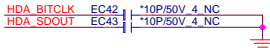




HDA

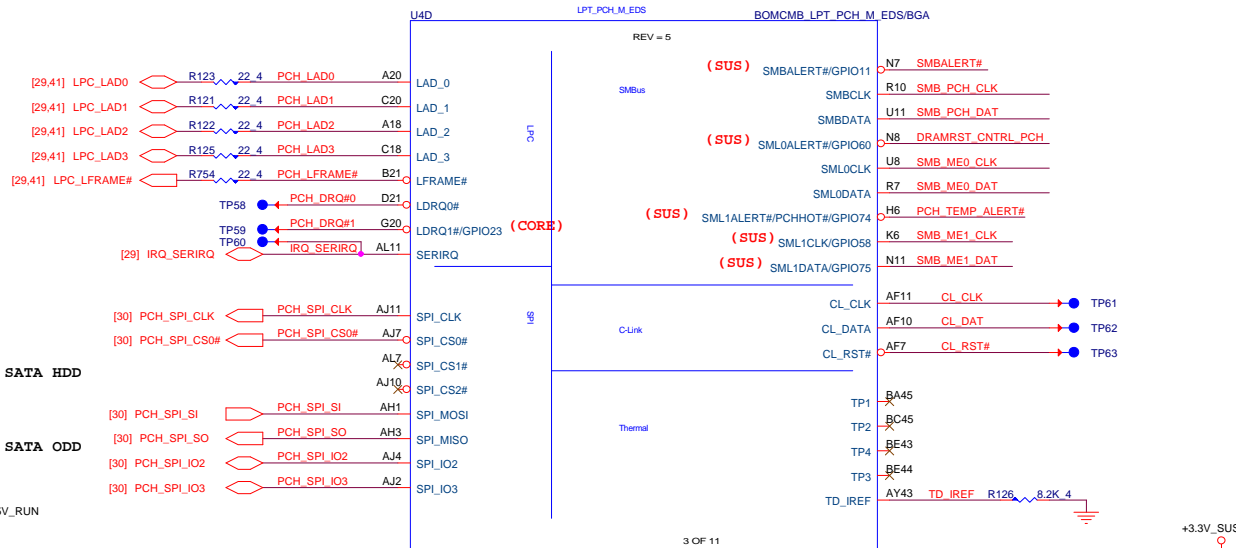


EMI



PCH STRAPPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	ACZ_SPKR R155 *1K 4 NC +3.3V_RUN
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	[12] SUSCLK R156 *1K 4 NC
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	[12] STP_A16OVR R159 *1K 4 NC
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R160 330K 4 +3V_RTC R714 330K 4 NC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Reserved 1 1 SPI 0 0 LPC	BBS_BIT0 R161 10K 4 +3.3V_RUN
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	[29] PCH_MELOCK 1K 4 R162 HDA_SDO_R
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	[12] DSWVREN R164 330K 4 +3V_RTC R165 330K 4 NC
GPIO53	DMI AC / DC-Coupling Mode	PWROK	0 = DMI is in AC-coupling mode 1 = DMI is in DC-coupling mode (int PU)	[12] PCH_GPIO53 R628 *1K 4 NC
HDA_DOCK_EN# / GPIO33	DMI TX Termination	PWROK	0 = DMI TX is terminated to VSS (Int PD) 1 = DMI TX is terminated to VCC/2.	PCH_GPIO33 R629 *1K 4 NC +3.3V_RUN

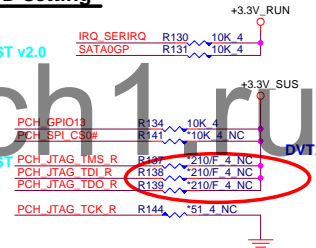


PCH PU/PD setting

Follow SCH CHKRSST v2.0

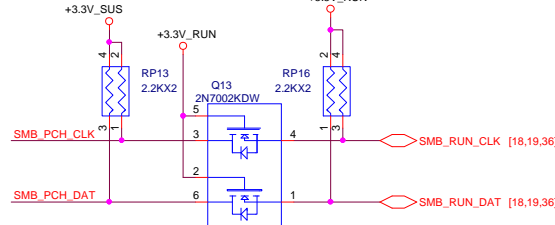
Follow DG v2.2

Follow SCH CHKRSST v2.0 pg27

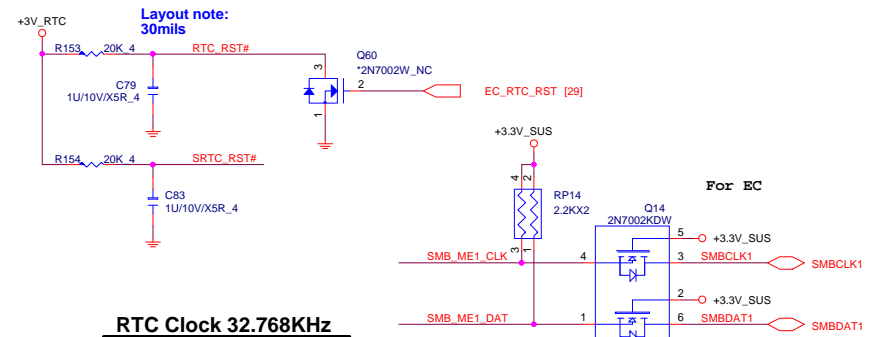


Leakage Isolation

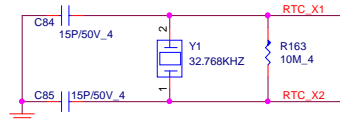
For DIMMs



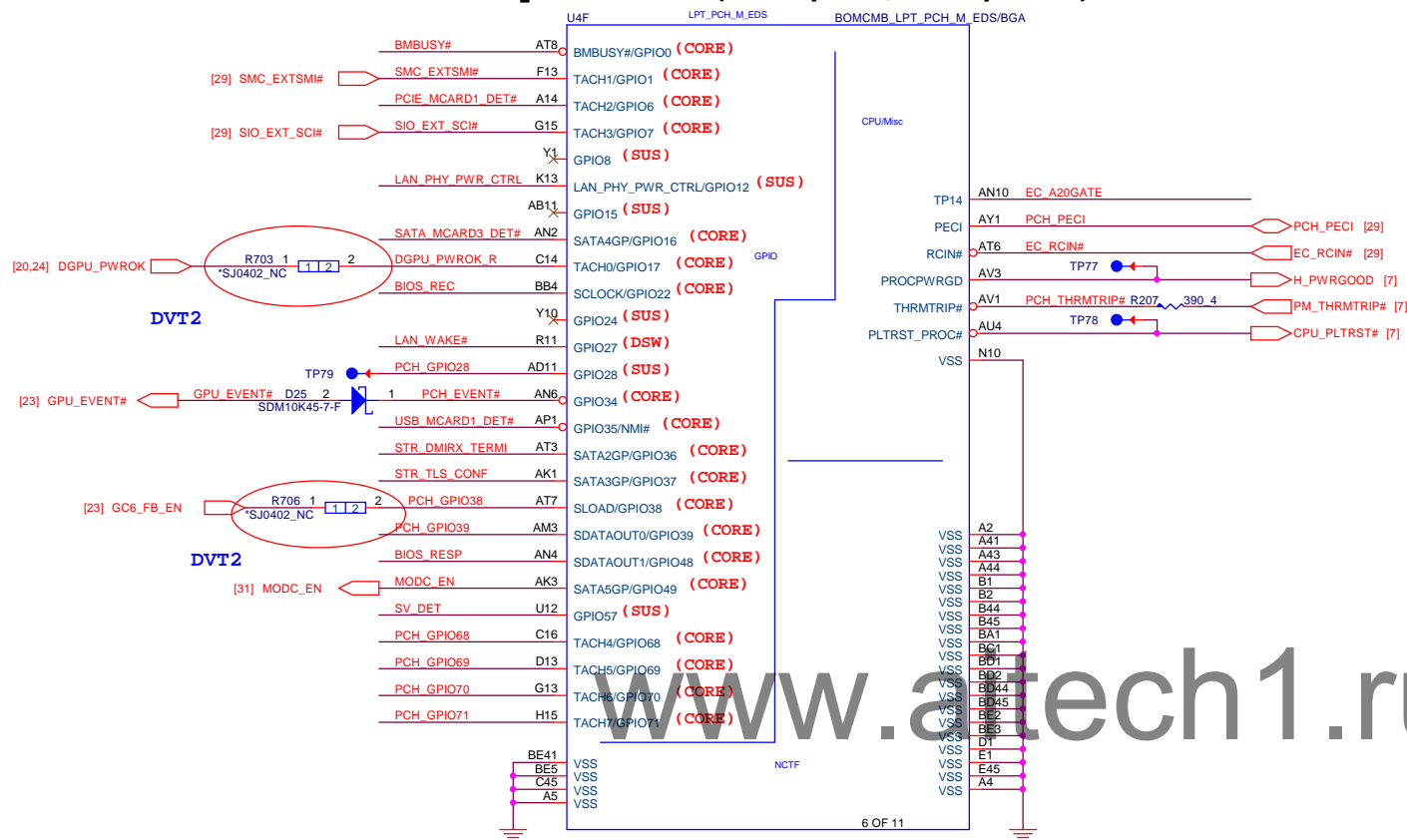
RTC Circuitry



RTC Clock 32.768KHz







LAN_WAKE# RP25 2 1 10KX2 +3.3V

LAN_PHY_PWR_CTRL 4 3

SMC_EXTSMI# RP24 2 1 10KX2 +3.3V

SIO_EXT_SCI# 4 3

EC_A20GATE RP27 2 1 10KX2

PCH_GPIO39 4 3

BMBSUSY# RP26 2 1 10KX4

EC_RSTN# 4 3

USB_MCARD1_DET# 6 5

SATA_MCARD3_DET# 8 7

PCH_GPIO69 RP5 2 1 10KX4

PCH_GPIO70 4 3

PCH_GPIO71 6 5

PCH_GPIO68 8 7

PCH_GPIO38 R212 10K 4 NC

DGPU_PWROK_R R615 10K 4

PCH_EVENT# R616 10K 4

PCIE_MCARD1_DET# R206 10K 4

SV_DET R223 100K 4

PCH Strap					
Pin Name	Usage	Sampled	Configuration	Ref. Doc.	Circuitry
SATA2GP / GPIO36	DMI RX Termination	Rising edge of PWROK	0 = DMI RX is terminated to VSS. 1 = DMI RX is terminated to VCC/2.	PCH EDS v2.3 SCH CHKLIST v2.0	
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	PCH EDS v2.3 SCH CHKLIST v2.0	

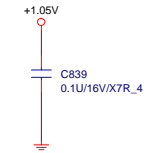
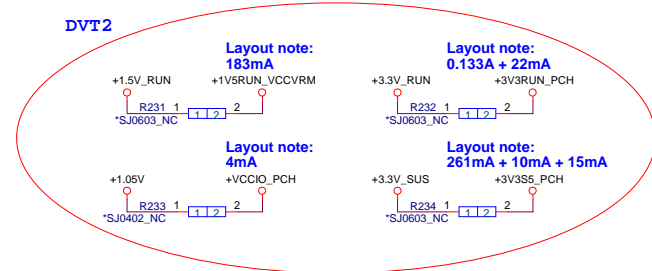
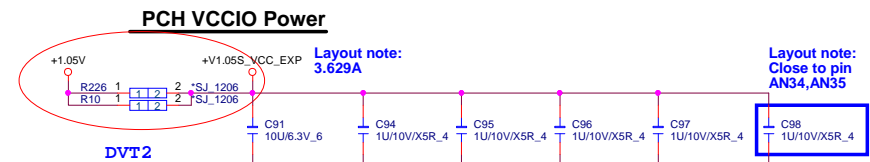
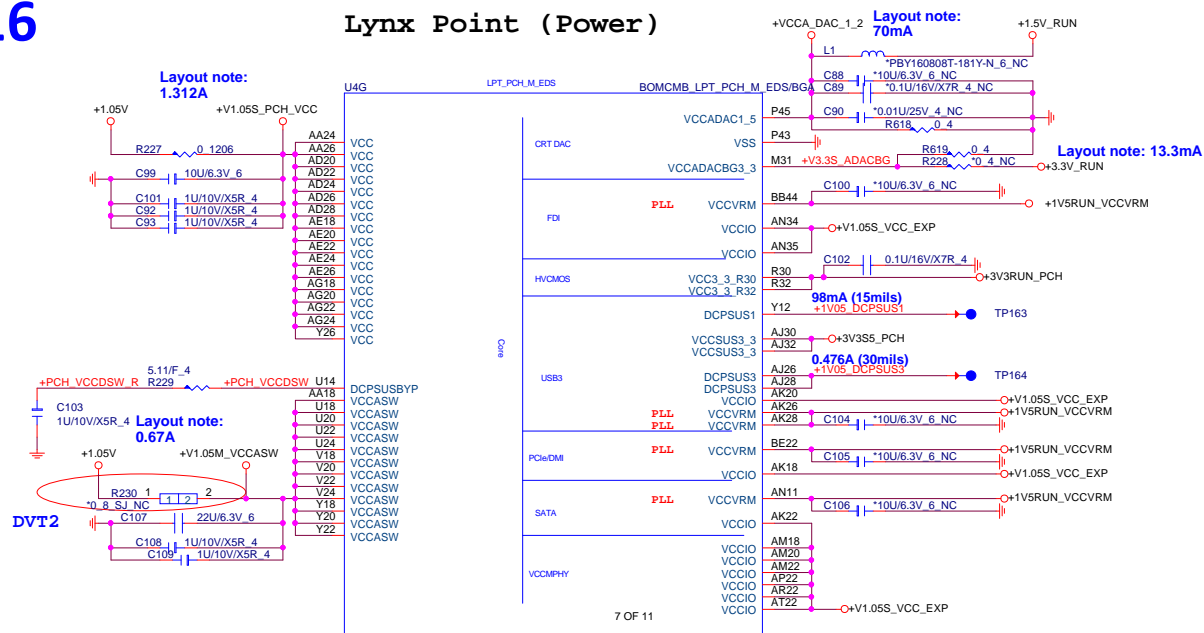
BIOS RECOVERY

0 = Enable
1 = Disable

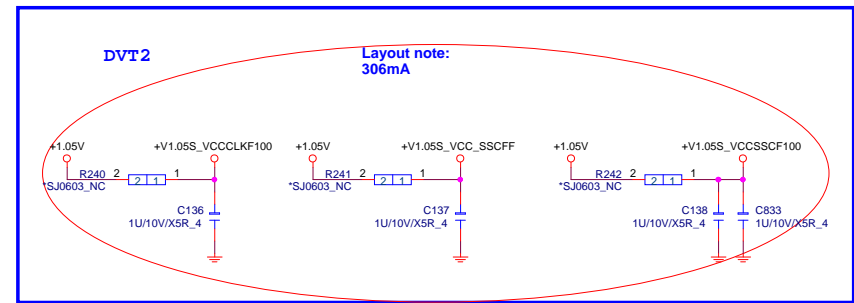
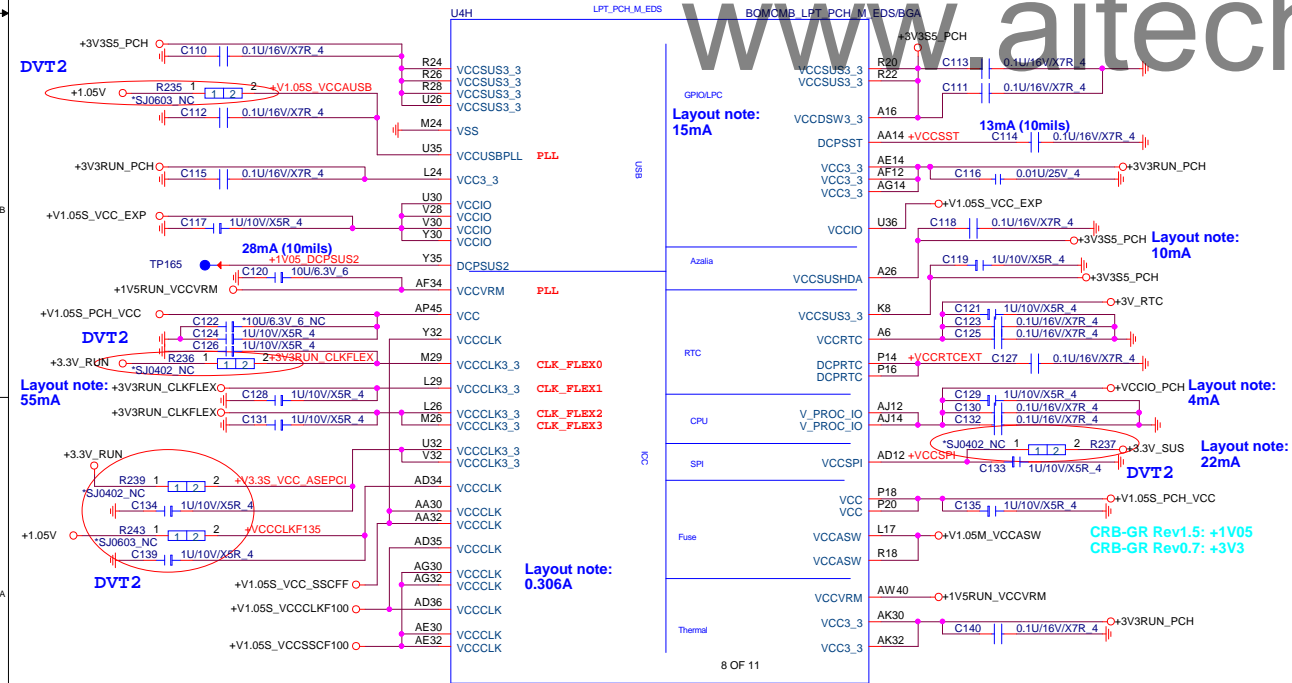
BIOS_RESP

0 = BIOS RESP
1 = Default

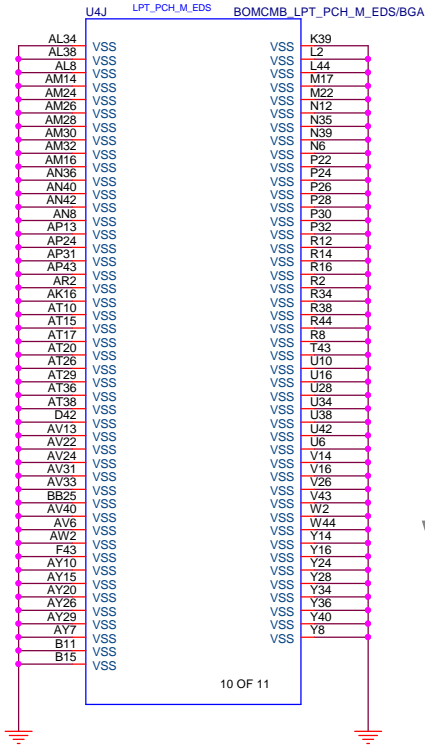
Lynx Point (Power)



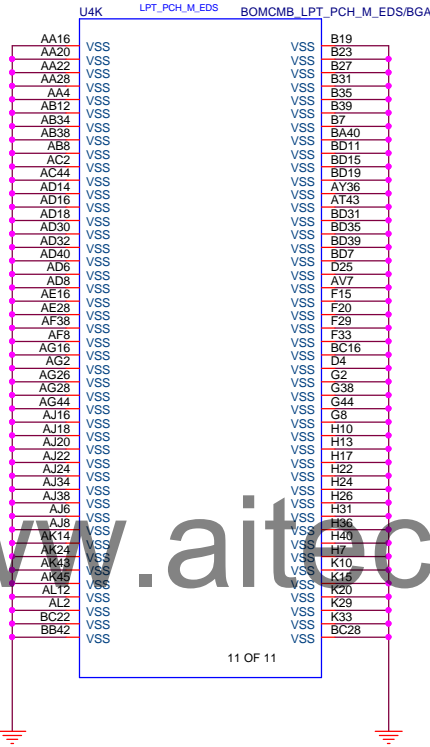
Lynx Point (Power)

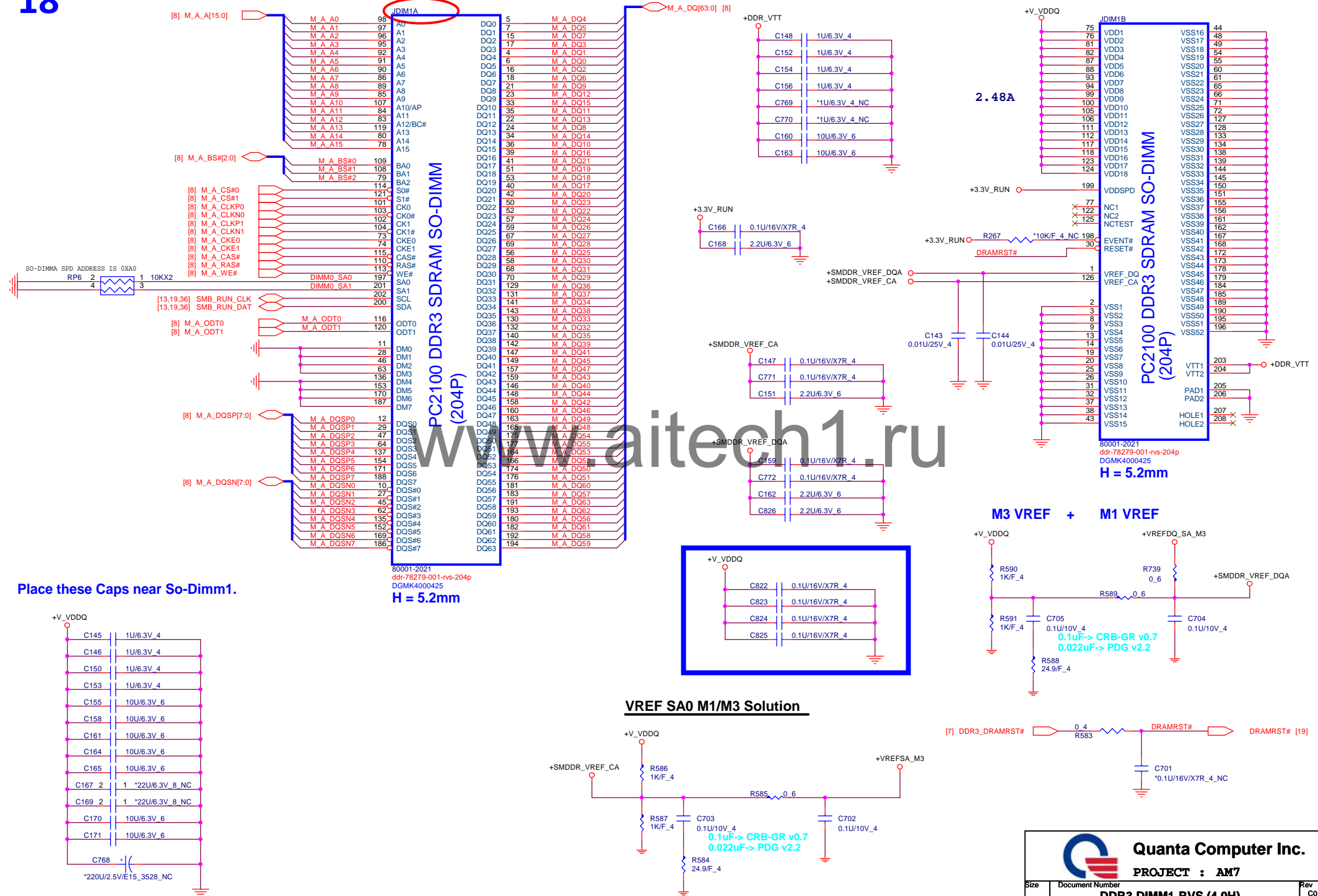


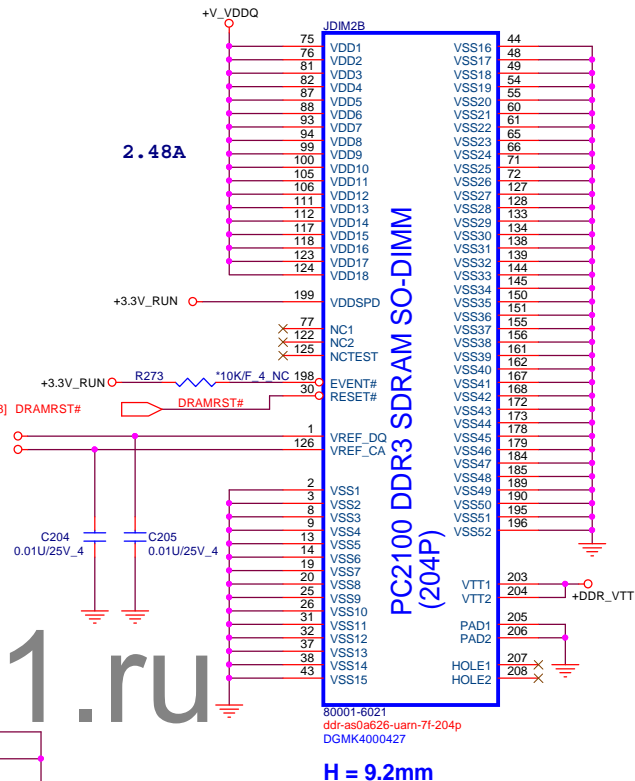
Lynx Point (GND)



Lynx Point (GND)

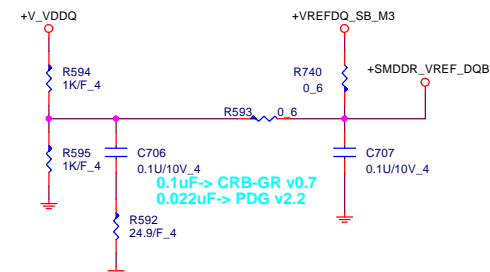
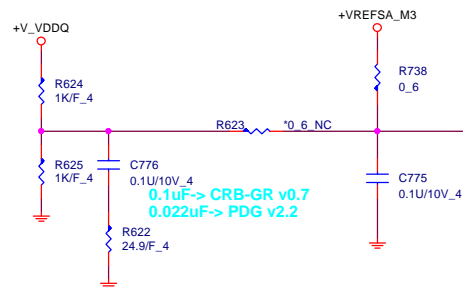


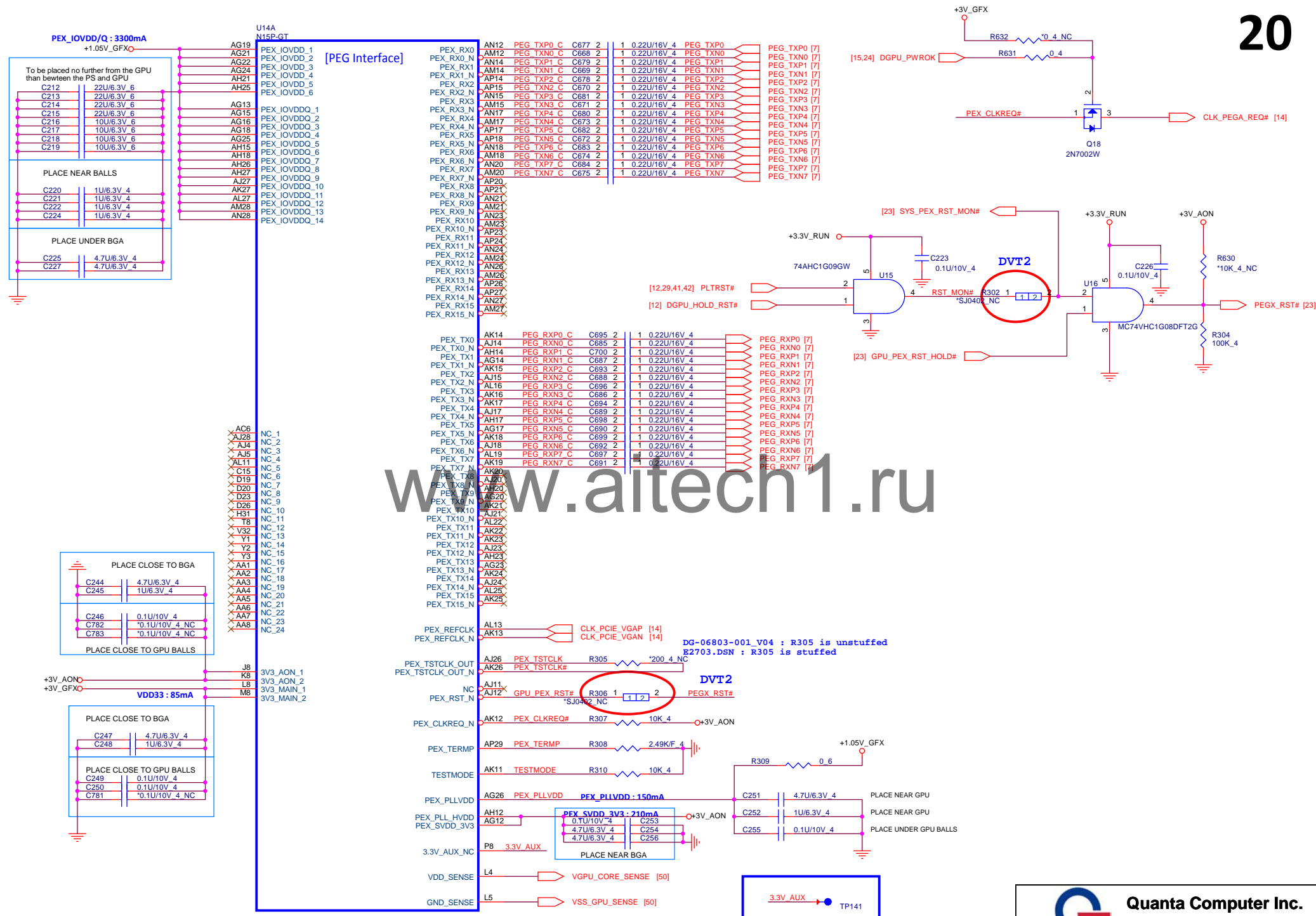


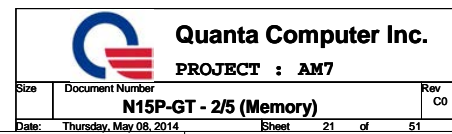


$H = 9.2\text{mm}$

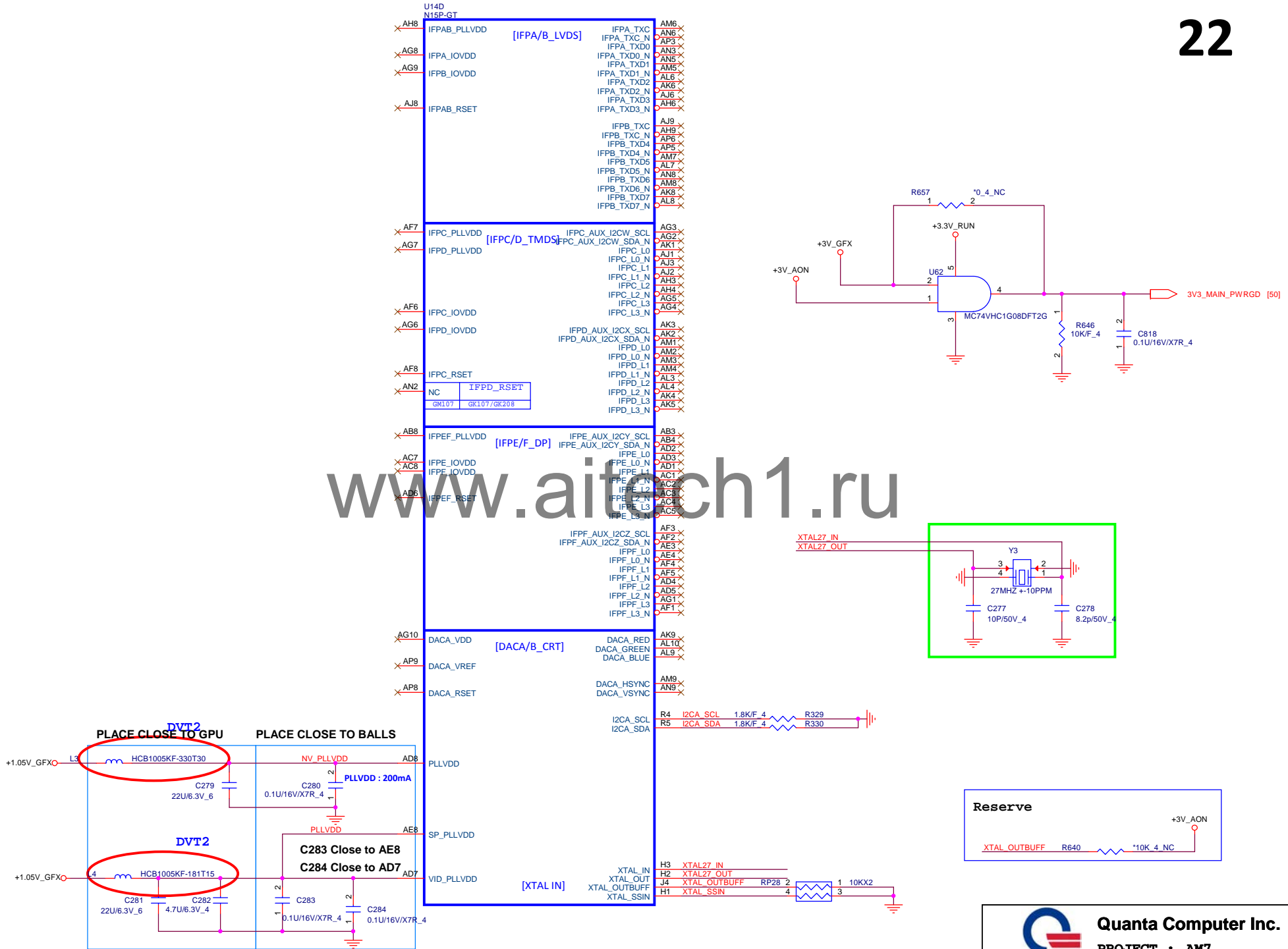
M3 VREF + M1 VREF







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[MIOA]

[MIOB]

[MISC_GPIO/I2C/JTAG/THER]

[MISC2_ROM]

BUFRST_N

OVERT

Default: Hynix 4G VRAM

Vendor	Q : P/N	Mfr. P/N	ROM_SI	
Hynix (1.35V)		H5TC4G63AFR-11C	0011	20K PD
Micron (1.35V)		MT41J256M16HA-093G:E	0100	24.9K PD
Samsung (1.35V)		K4W4G1646D-BC1A	0101	30.1K PD

N15P-GT device ID= 0x1391		
Netname	N15P-GT	
ROM_SCLK	4.99K PD	0000
ROM_SO	4.99K PD	0000
STRAP0	45.3K PU	

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1%(0402)
 24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1%(0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1%(0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

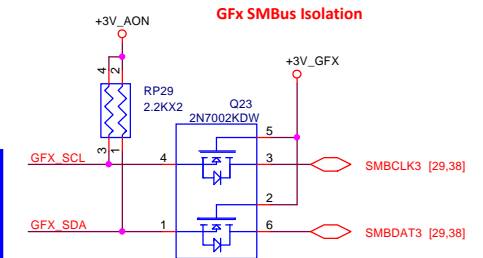
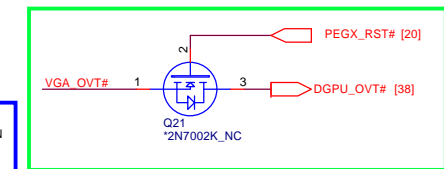
Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50K pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			
STRAP2				
STRAP3				
STRAP4				

Table 28. N155-GX and N15P-GT DDR3L Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDDQ/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3L	Hynix	0x3	1.35 V/ 1.35 V	H5TC4G63AFR-11C	900	N/A	Production candidate
	Micron	0x4	1.35 V/ 1.35 V	MT41J256M16HA-093G:E	900	1322	Production candidate
	Samsung	0x5	1.35V/ 1.35V	K4W4G1646D-BC1A	900	N/A	Post-production candidate

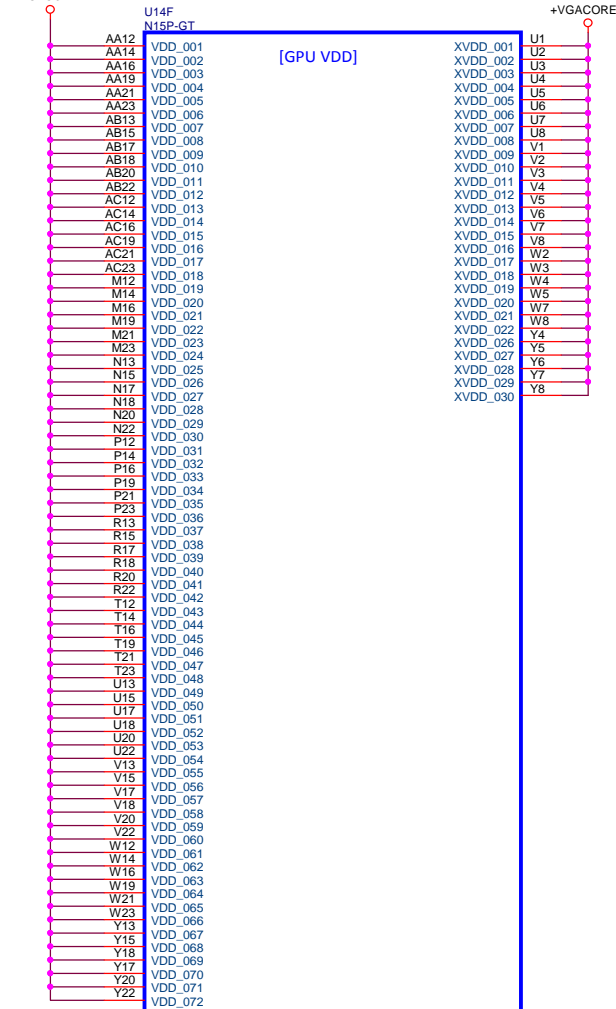
Note: For N155-GX and N15P-GT, the maximum allowable memory case temperature is 85 °C.



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VDD/XVDD : 43A

+VGACORE

U14G
N15P-GT

A2

AA17

AA18

AA20

AA22

AB12

AB14

AB16

AB19

AB21

AB23

AB28

AB30

AB32

AB5

AC13

AC15

AC17

AC18

AA13

AC20

AC22

AE2

AE28

AE30

AE32

AE33

AE5

AE7

AH10

AA15

AH13

AH16

AH19

AH2

AH22

AH24

AH28

AH29

AH30

AH32

AH33

AH5

AH7

AJ7

AK10

AK7

AL12

AL14

AL15

AL17

AL18

AL2

AL20

AL21

AL23

AL24

AL26

AL28

AL30

AL32

AL33

AL5

AM13

AM16

AM19

AM22

AM25

AN1

AN10

AN13

AN16

AN19

AN22

AN25

AN30

AN34

AN4

AP2

AP33

B1

B10

B22

B25

B28

B31

B34

B4

B7

C10

C13

C19

C22

C25

C28

C7

GND_100

[GPU GND]

GND_101

GND_102

GND_103

GND_104

GND_105

GND_106

GND_107

GND_108

GND_109

GND_110

GND_111

GND_112

GND_113

GND_114

GND_115

GND_116

GND_117

GND_118

GND_119

GND_120

GND_121

GND_122

GND_123

GND_124

GND_125

GND_126

GND_127

GND_128

GND_129

GND_130

GND_131

GND_132

GND_133

GND_134

GND_135

GND_136

GND_137

GND_138

GND_139

GND_140

GND_141

GND_142

GND_143

GND_144

GND_145

GND_146

GND_147

GND_148

GND_149

GND_150

GND_151

GND_152

GND_153

GND_154

GND_155

GND_156

GND_157

GND_158

GND_159

GND_160

GND_161

GND_162

GND_163

GND_164

GND_165

GND_166

GND_167

GND_168

GND_169

GND_170

GND_171

GND_172

GND_173

GND_174

GND_175

GND_176

GND_177

GND_178

GND_179

GND_180

GND_181

GND_182

GND_183

GND_184

GND_185

GND_186

GND_187

GND_188

GND_189

GND_190

GND_191

GND_192

GND_193

GND_194

GND_195

GND_196

GND_197

GND_198

GND_199

GND_200

GND_OPT_1

GND_OPT_2

D2

D31

D33

E10

E22

E25

E5

E7

F28

G10

G13

G16

G19

G2

G22

G25

G28

G3

G30

G32

G33

G5

G7

K2

K28

K30

K32

K33

K6

K7

M13

M15

M17

M18

M20

M22

N12

N14

N16

N19

N2

N23

N28

N30

N32

N33

N5

N7

P13

P15

P17

P18

P20

P22

R12

R14

R16

R19

R21

R23

R15

T17

T18

T2

T20

T22

AG11

T28

T32

T5

T7

U12

U14

U16

U19

U21

U23

U14

V12

V14

V16

V19

V21

V23

W13

W15

W17

W18

W20

W22

W28

Y12

Y14

Y16

Y19

Y21

Y23

AH11

+VGACORE

C286

C287

C288

C289

C290

C291

C292

C293

C294

C295

C296

C297

C298

C299

C300

C301

C302

C303

C304

C305

C306

C307

C308

C26

C27

C28

C29

C30

C31

C32

C316

C317

C318

C319

C320

C32

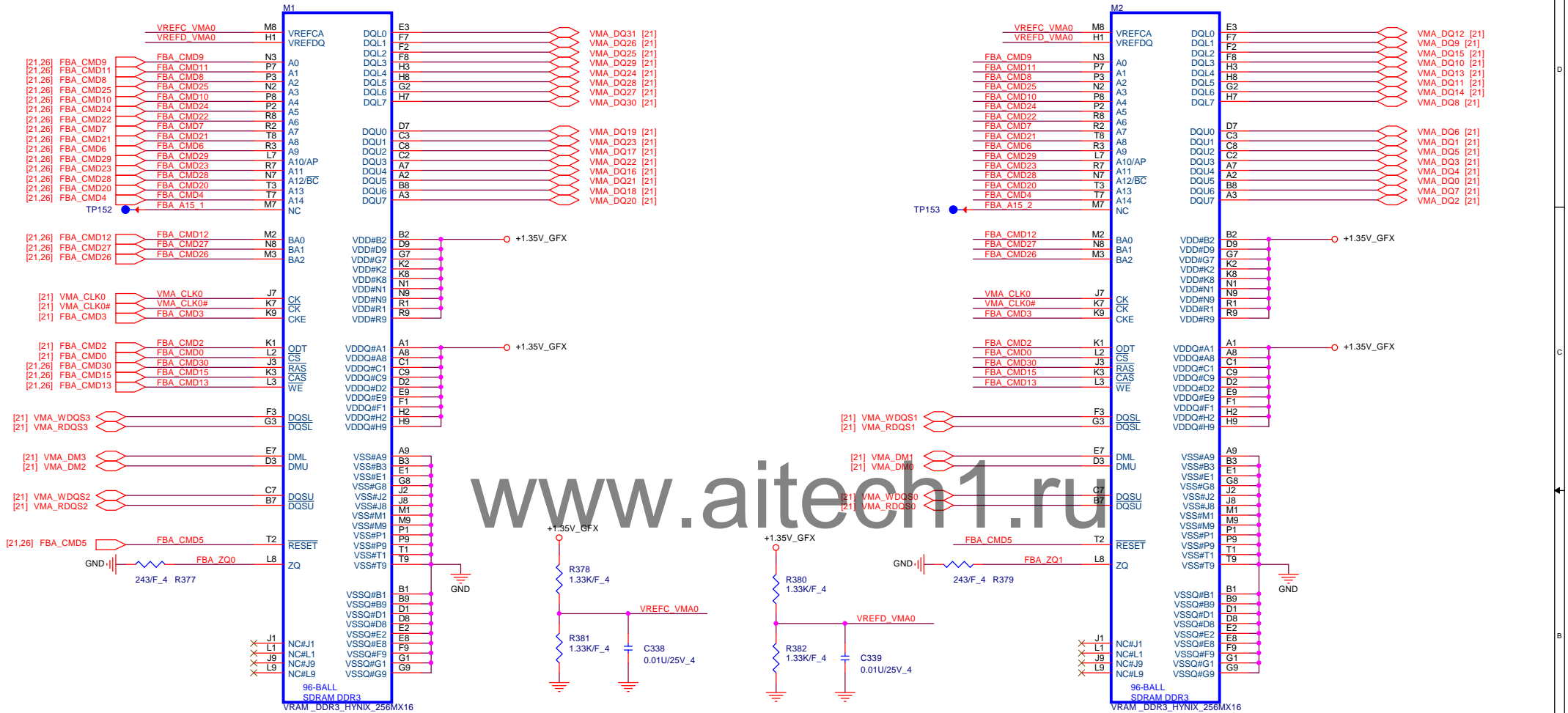
C316

C317

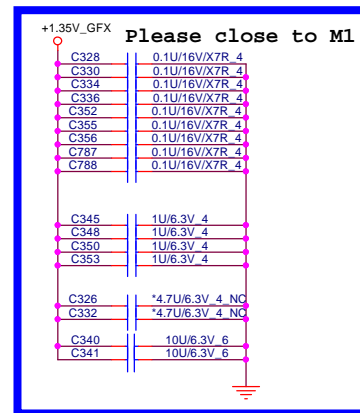
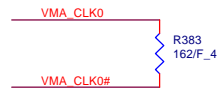
C318

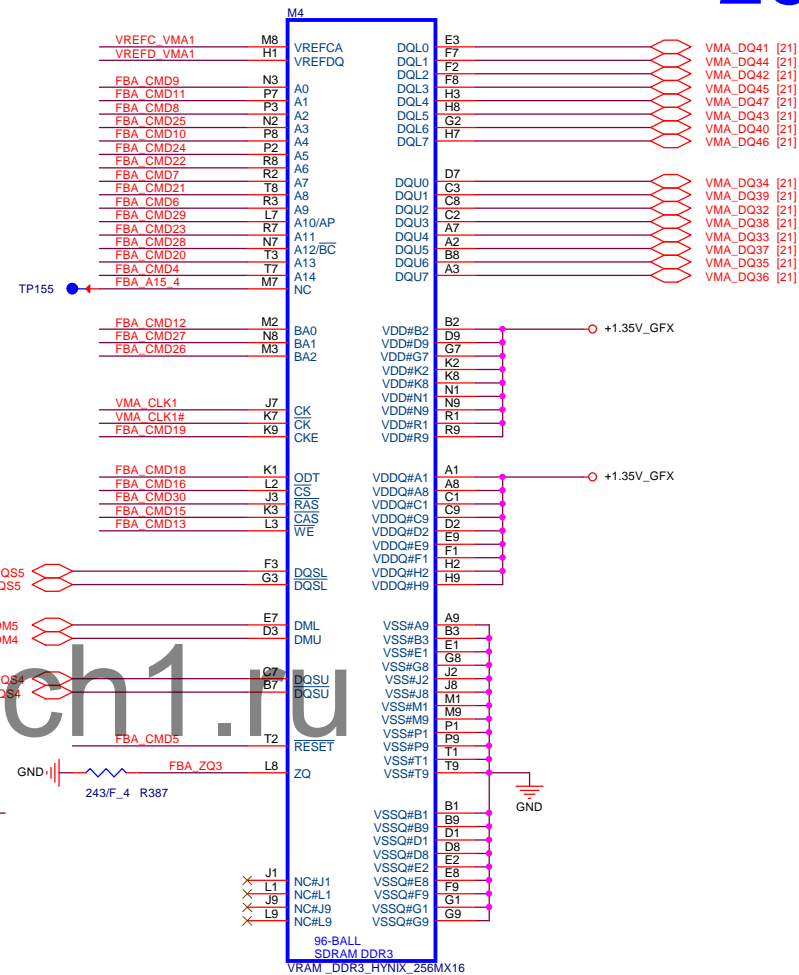
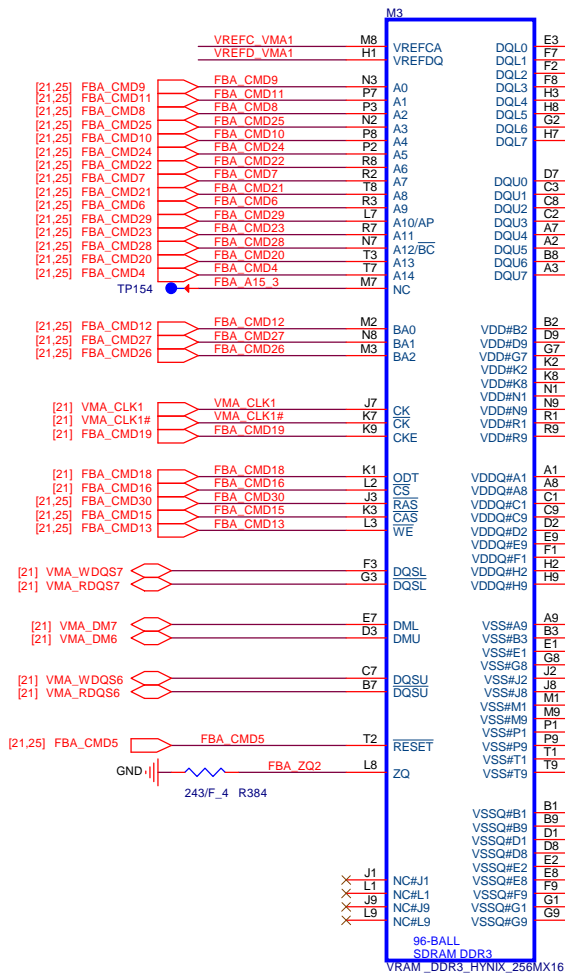
C319

HYU 256Mx16, H5TC4G63APR-11C QBC PN : AKD5PGWTW05---WINBSQ PN : AKD5PGWTW11
 MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL02---WINBSQ PN :
 SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT500---WINBSQ PN : NO

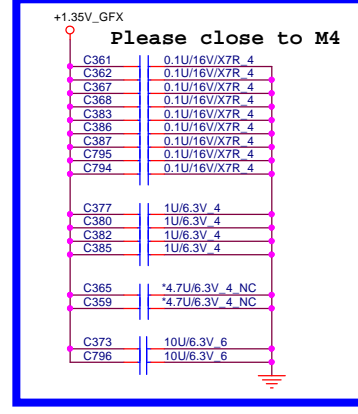
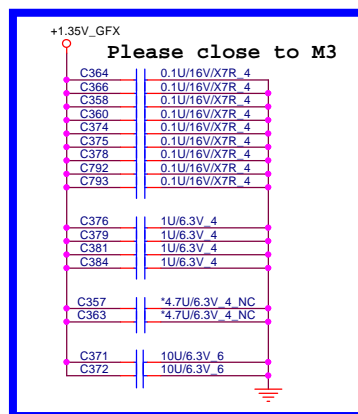
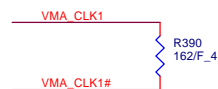


162_1 ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
 CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

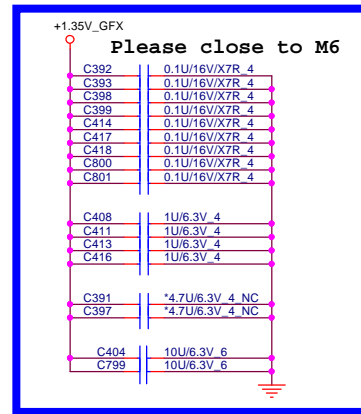


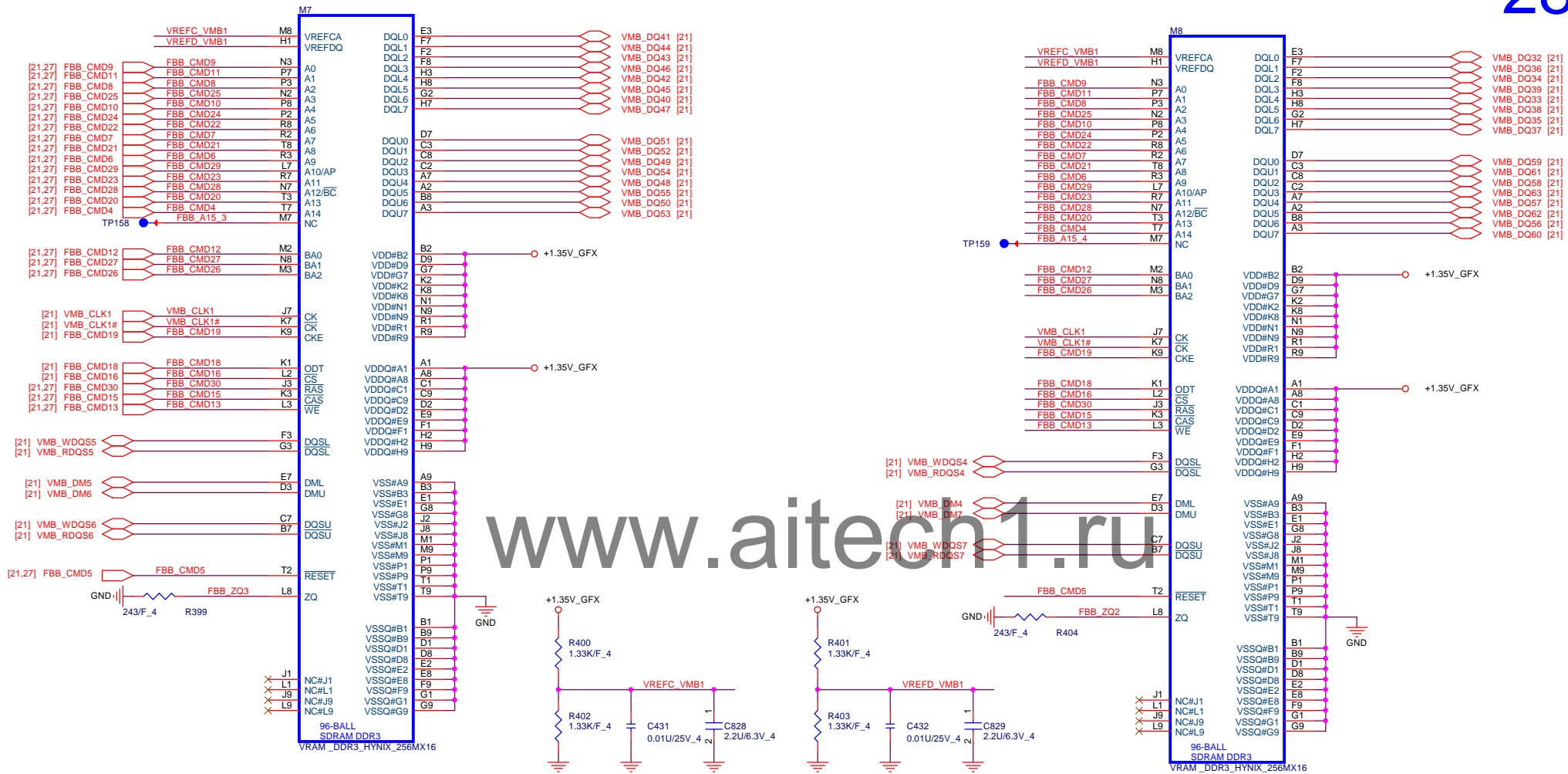


162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

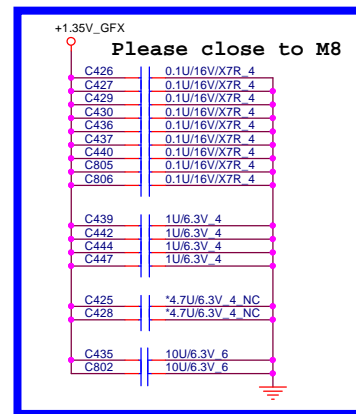
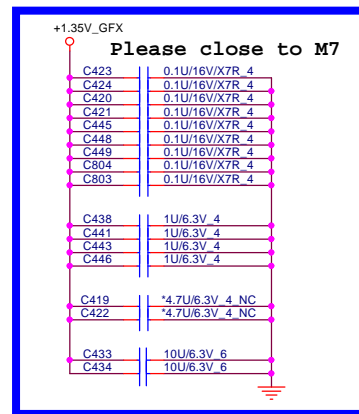
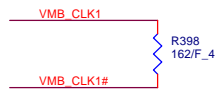


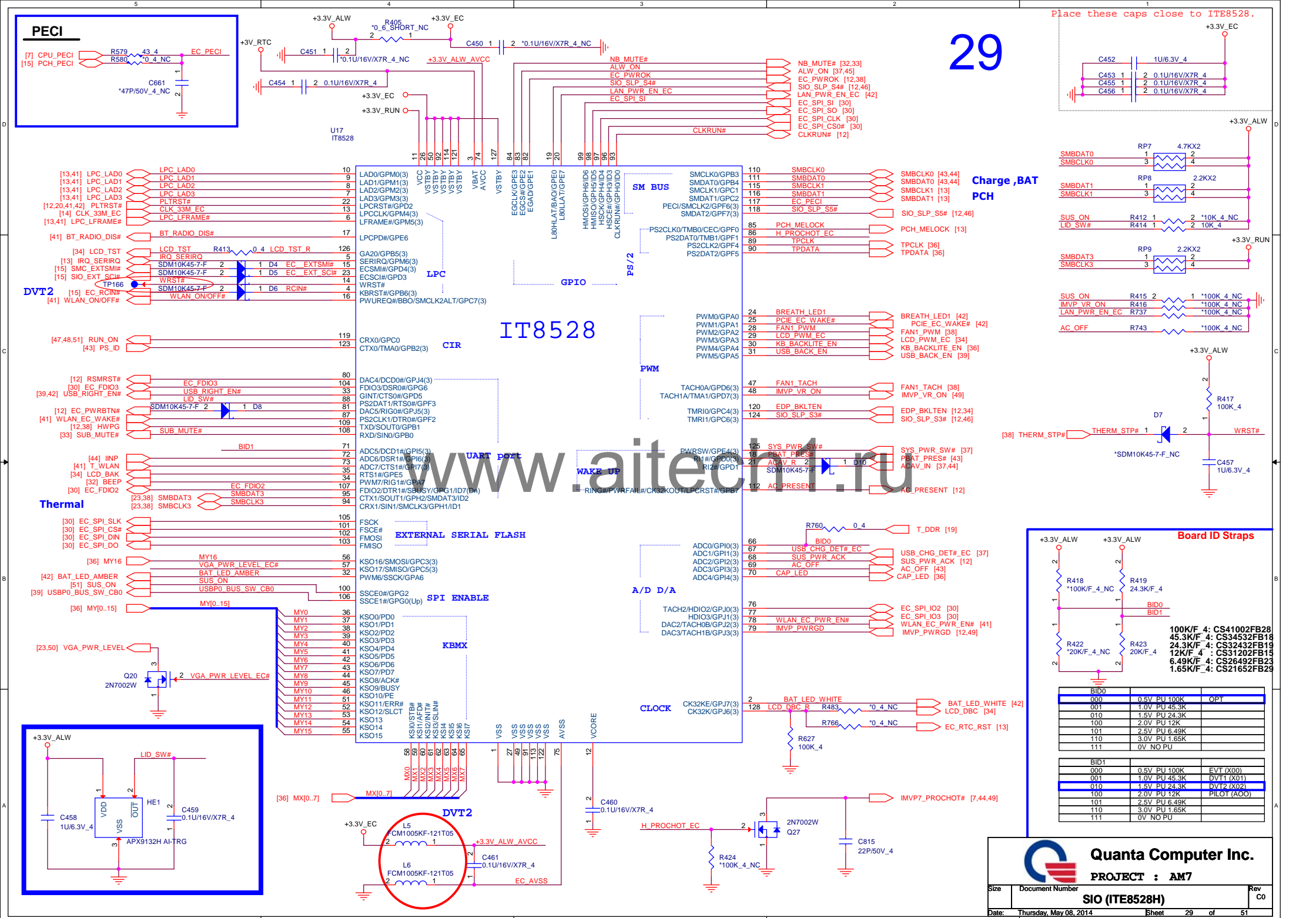
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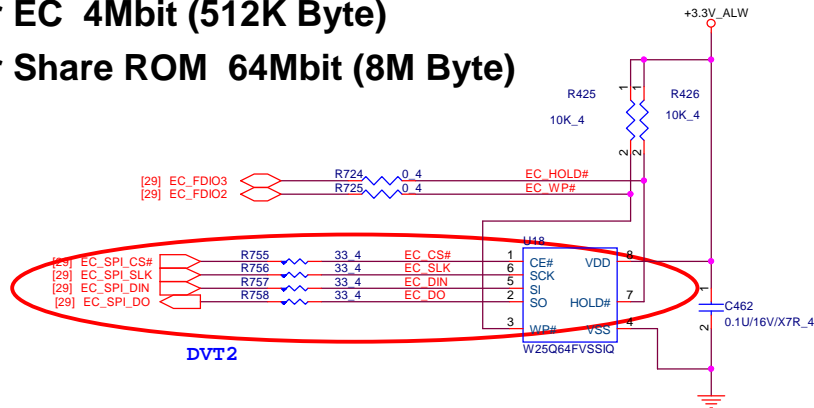


162_1k ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)





For EC 4Mbit (512K Byte)
For Share ROM 64Mbit (8M Byte)

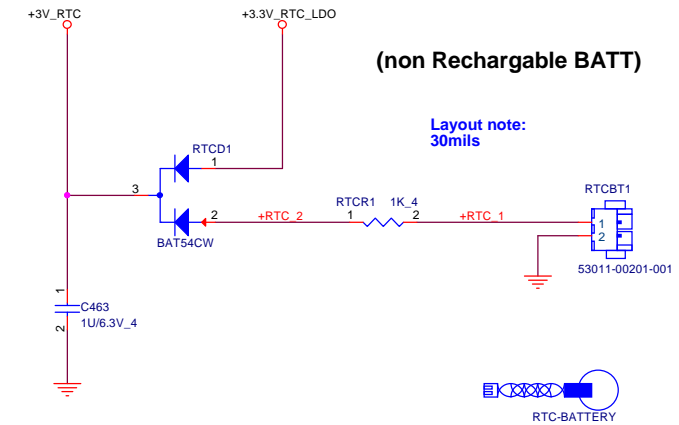


RTC BATTERY

30

(non Rechargeable BATT)

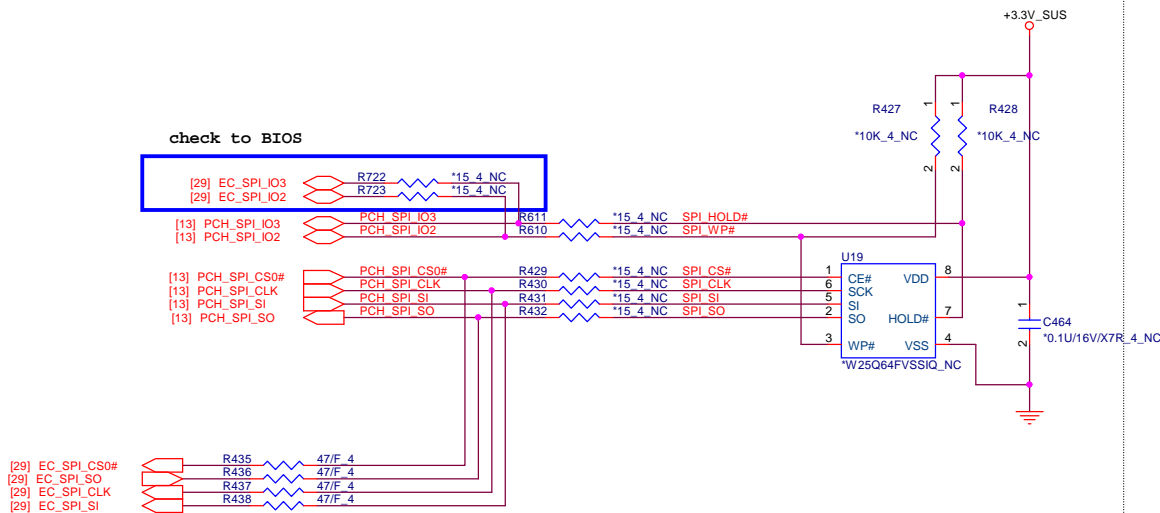
Layout note:
30mils



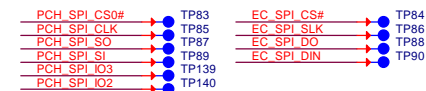
For PCH 32Mbit (4M Byte)

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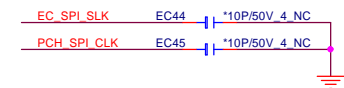
check to BIOS



TP for ICT flash BIOS process



EMI

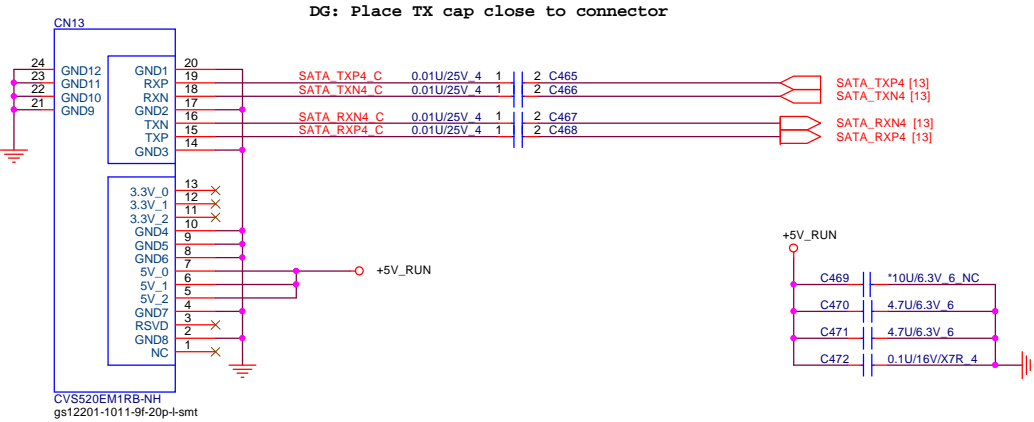


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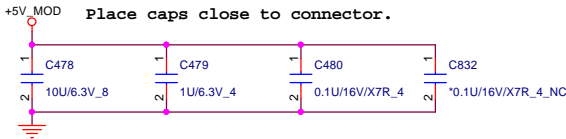
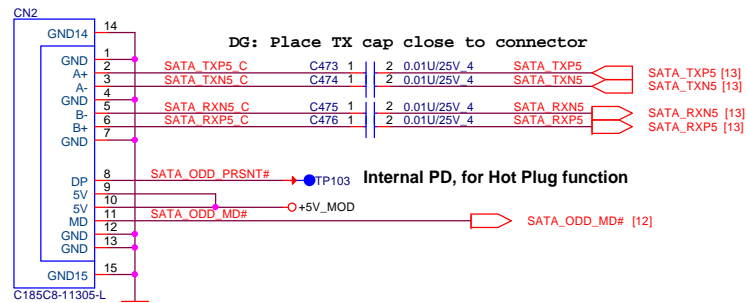
FLASH / RTC

SATA HDD Connector

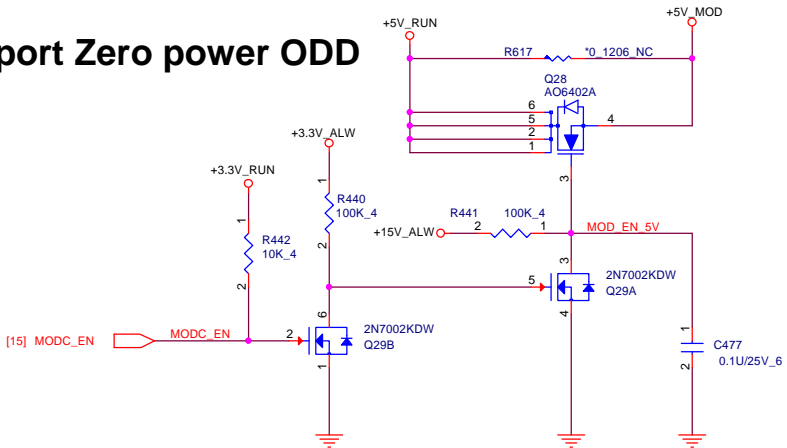


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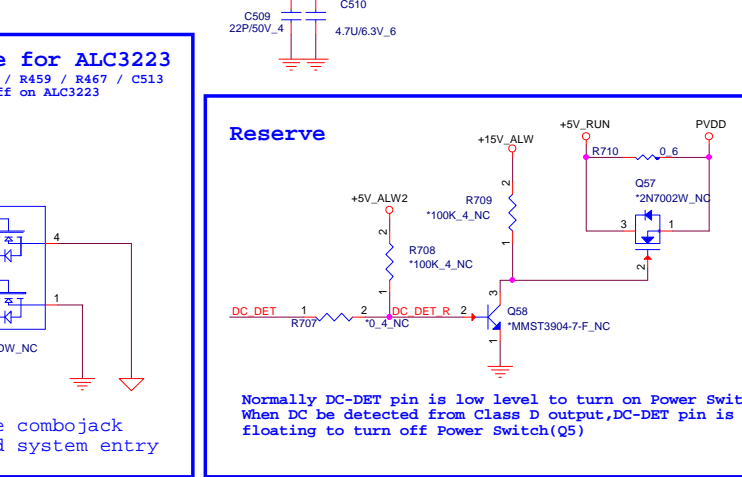
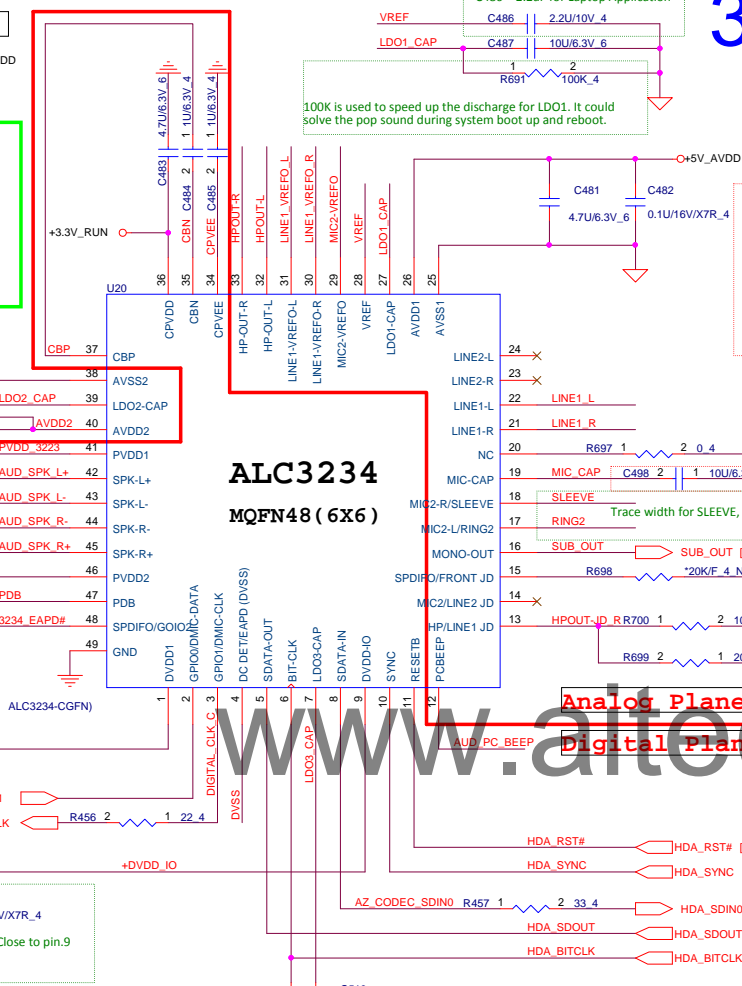
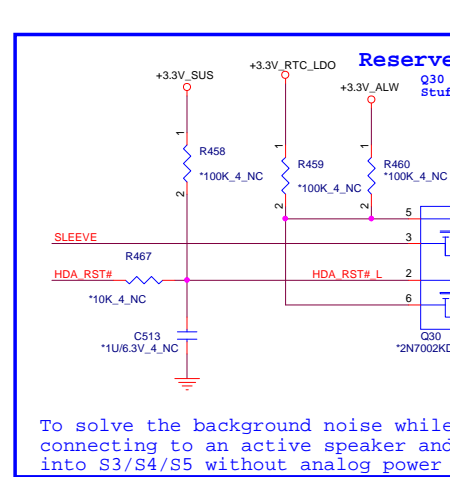
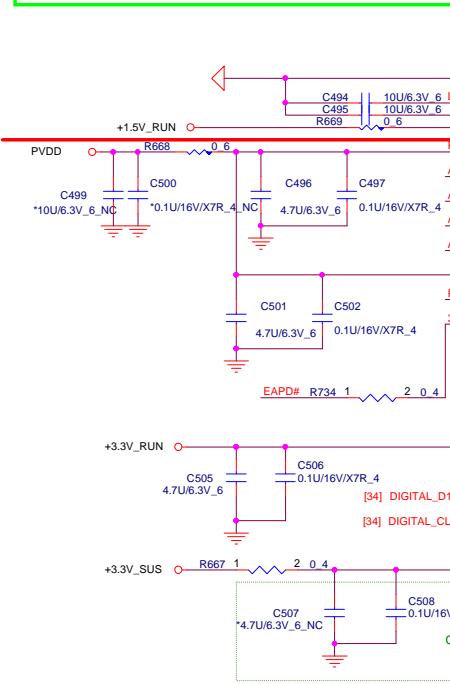
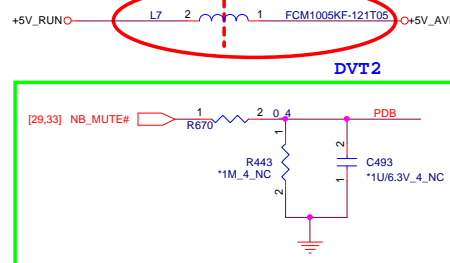
ODD



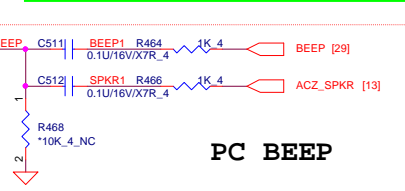
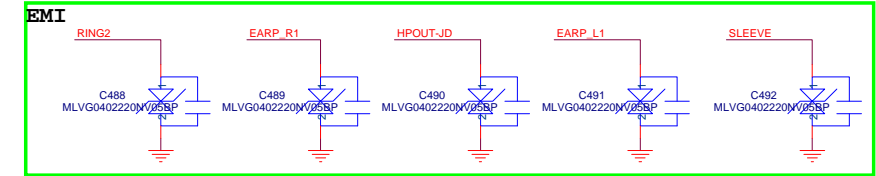
Support Zero power ODD



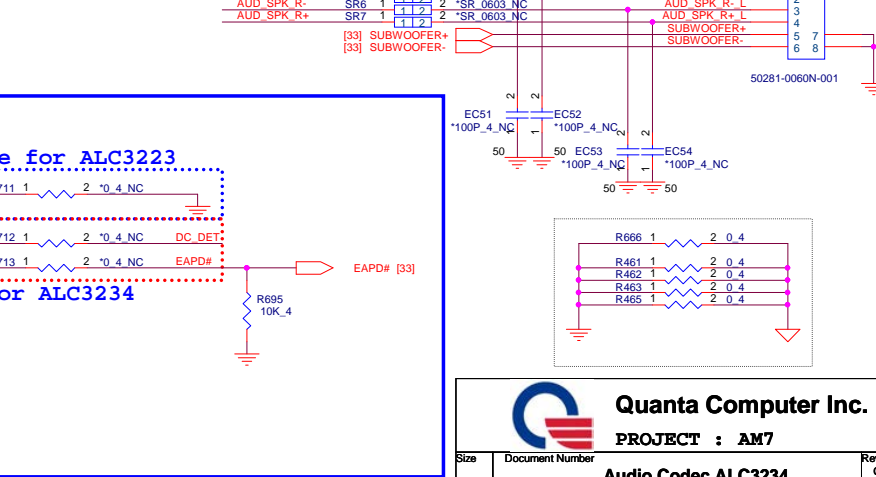
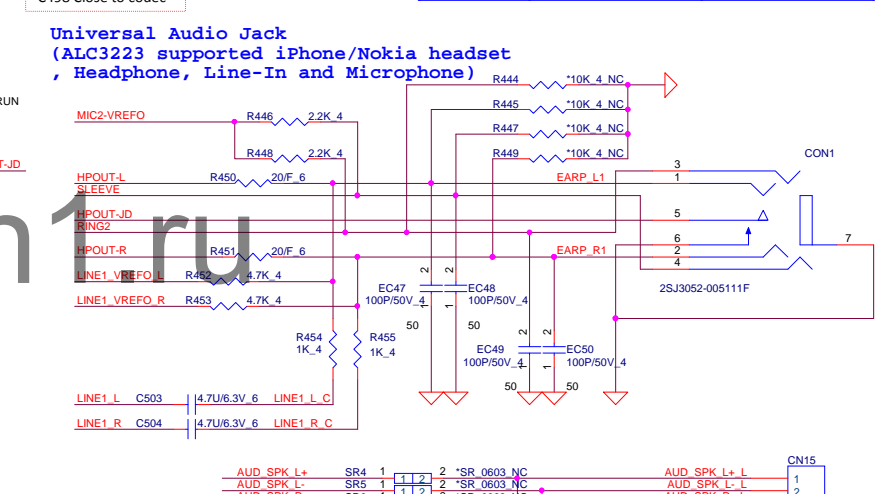
Digital Plane Analog Plane



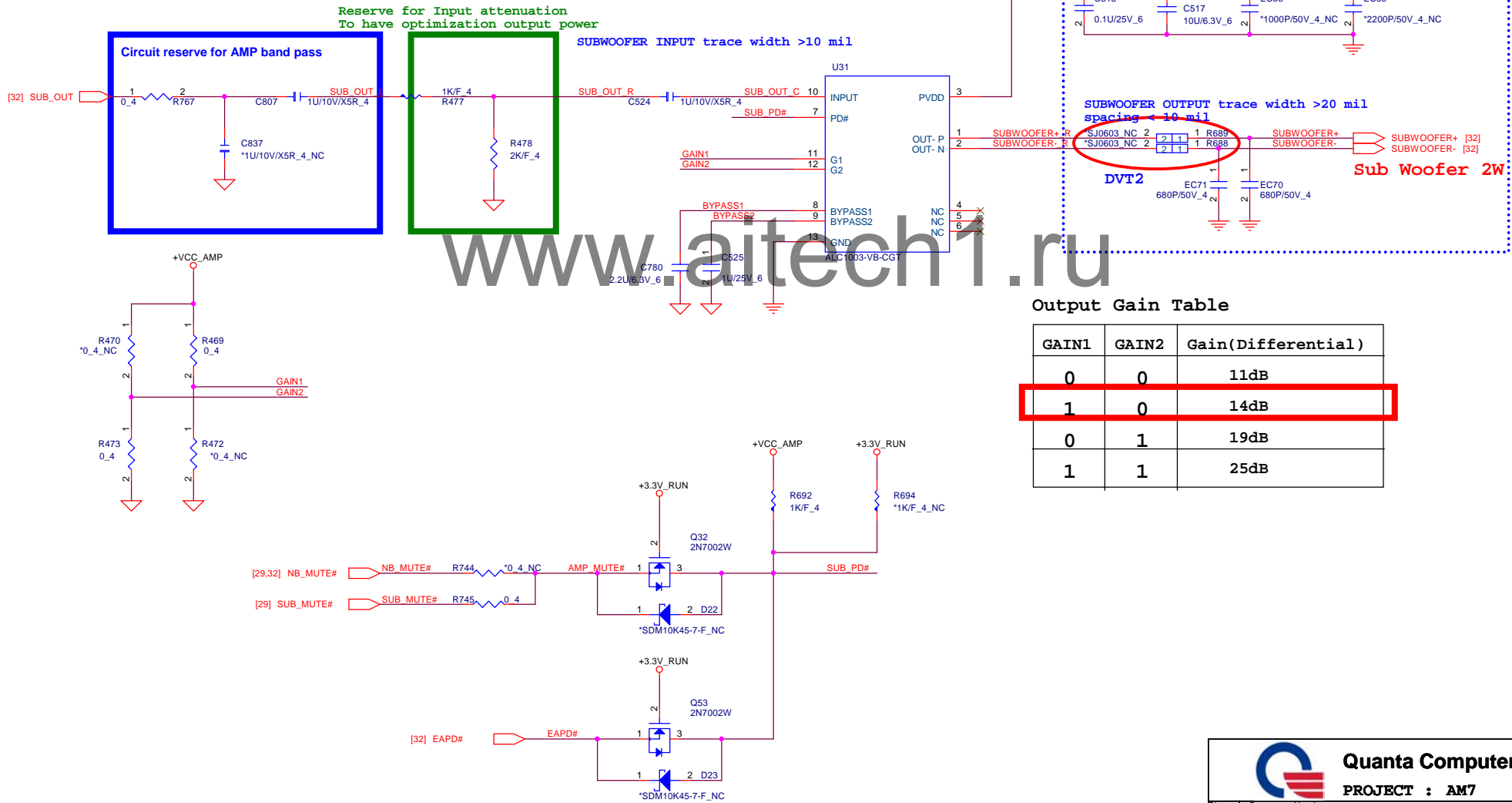
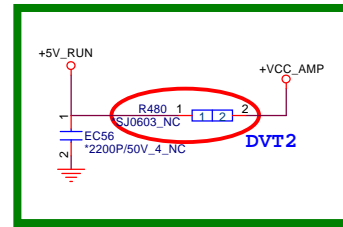
32



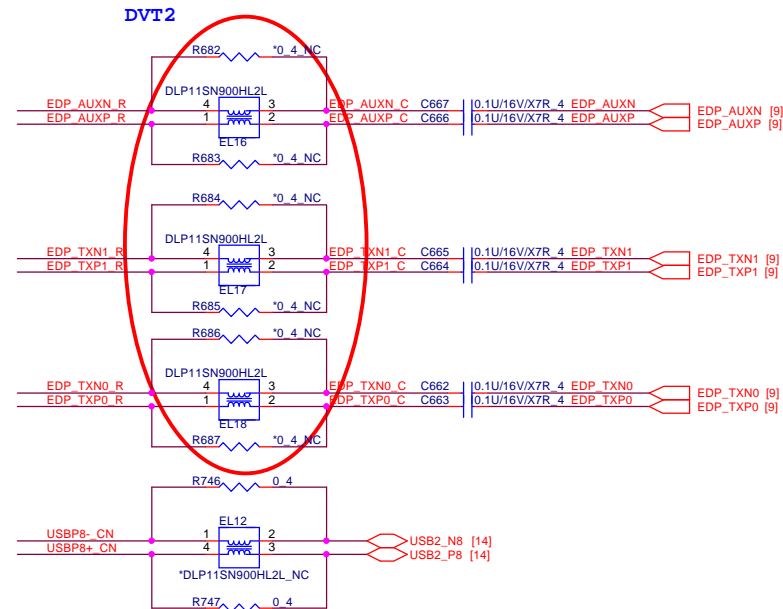
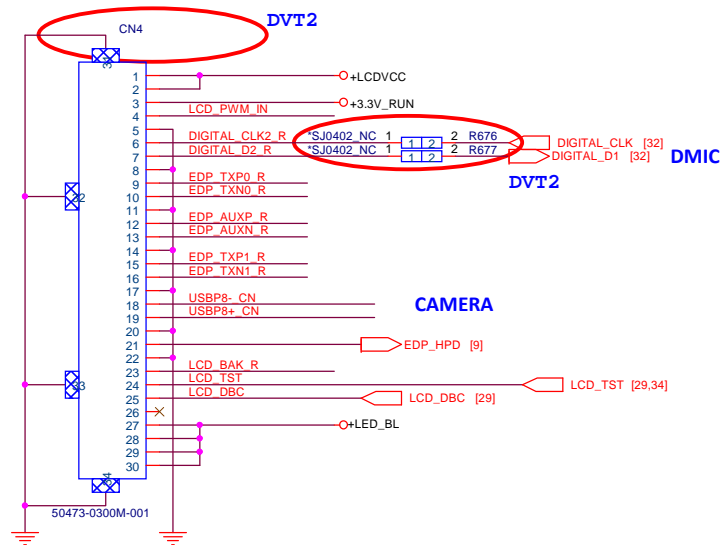
Parts	ALC3234 N/A	ALC3223 AL003223000
R697	0Ω	NC
R698	NC	20KΩ 1% CS32002FB29
R699	200KΩ 5% CS42002FB12	39.2KΩ 1% CS33922FB15
R700	100KΩ 5% CS41002JB20	NC
R734	0Ω	NC



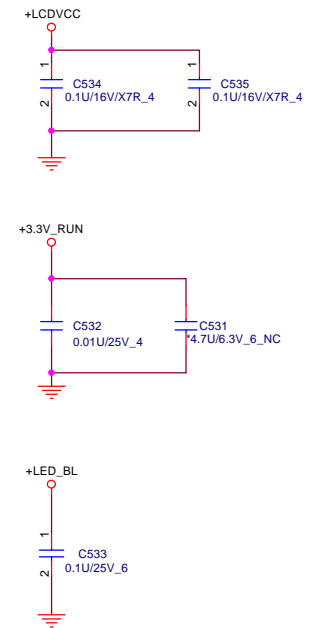
Subwoofer Amp



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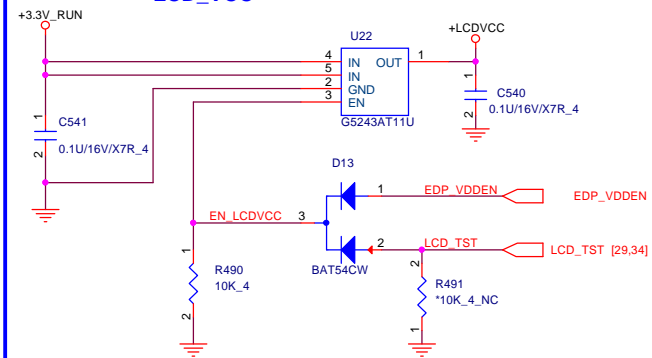


Close to CN4

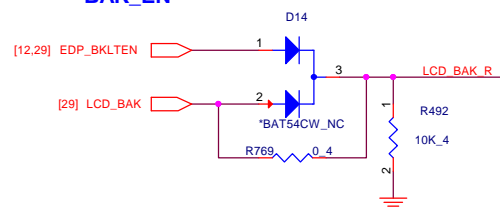


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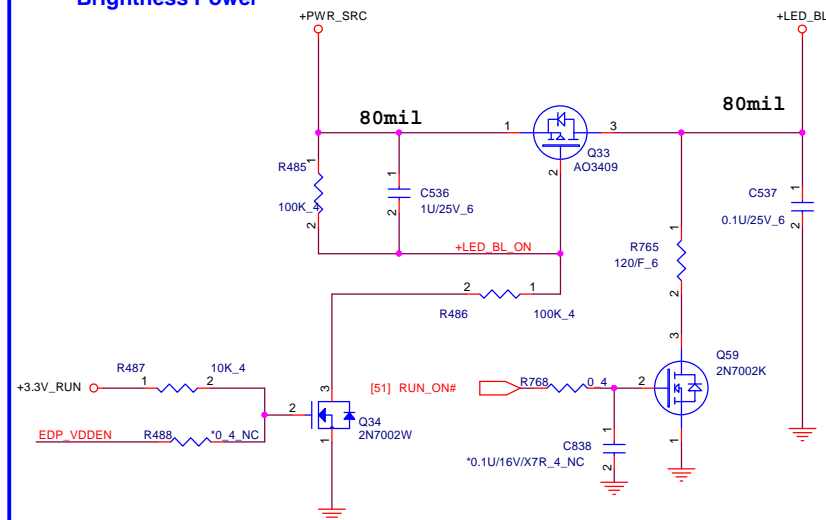
LCD_VCC



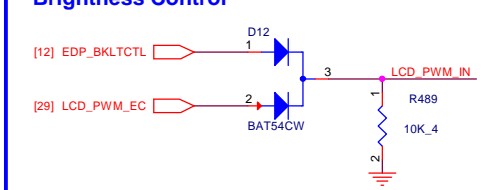
BAK_EN



Brightness Power



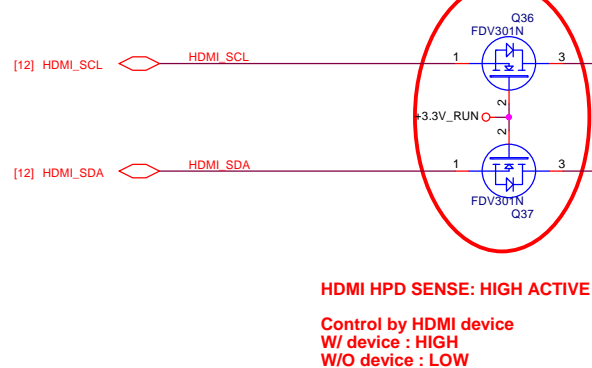
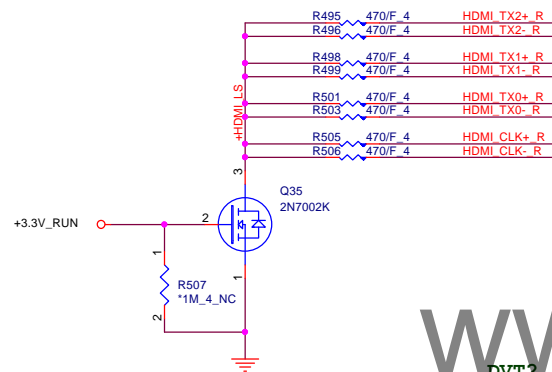
Brightness Control



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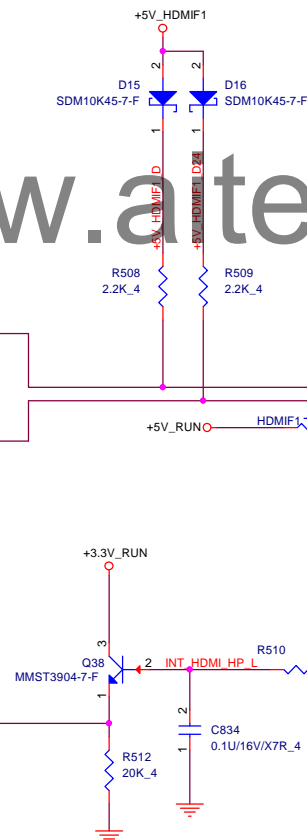
INT HDMI

[9]	INT_HDMI_TXP2	INT HDMI TXP2	C542	1	2	0.1U/16V/X7R	4	HDMI TX2+ R
[9]	INT_HDMI_TXN2	INT HDMI TXN2	C543	1	2	0.1U/16V/X7R	4	HDMI TX2- R
[9]	INT_HDMI_TXP1	INT HDMI TXP1	C544	1	2	0.1U/16V/X7R	4	HDMI TX1+ R
[9]	INT_HDMI_TXN1	INT HDMI TXN1	C545	1	2	0.1U/16V/X7R	4	HDMI TX1- R
[9]	INT_HDMI_TXP0	INT HDMI TXP0	C546	1	2	0.1U/16V/X7R	4	HDMI TX0+ R
[9]	INT_HDMI_TXN0	INT HDMI TXN0	C547	1	2	0.1U/16V/X7R	4	HDMI TX0- R
[9]	INT_HDMI_TXCP	INT HDMI TXCP	C548	1	2	0.1U/16V/X7R	4	HDMI CLK+ R
[9]	INT_HDMI_TXCN	INT HDMI TXCN	C549	1	2	0.1U/16V/X7R	4	HDMI CLK- R



HDMI HPD SENSE: HIGH ACTIVE

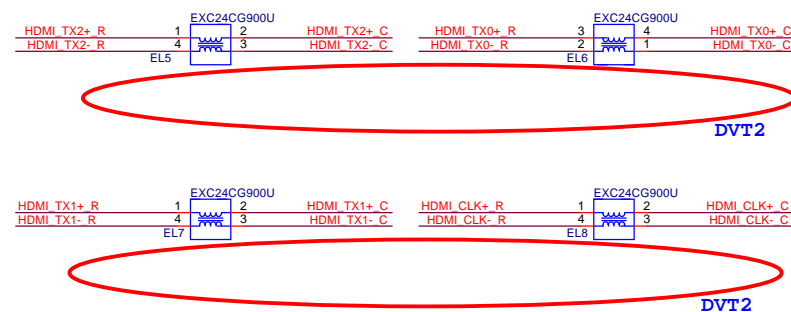
Control by HDMI device
W/ device : HIGH
W/O device : LOW



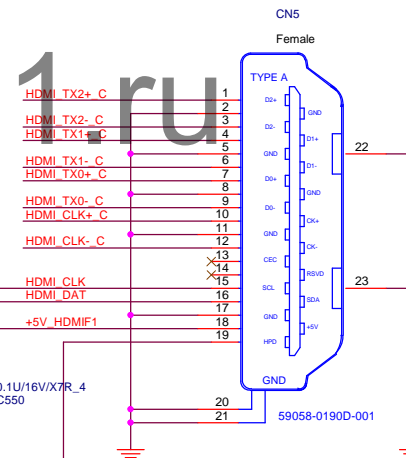
```
Ib = ( Vb - Vbe<sat> ) / Rb
Ic = ( Vc - Vce<sat> ) / Rc
Ib >> ( Ic / 40~70 )

(3.3-0.25)/20 = 152.5uA
152.5/ 40~70 = 3.8125 ~2.179 uA
(2.9-2.1)/ 3.8125 = 183.6K
```

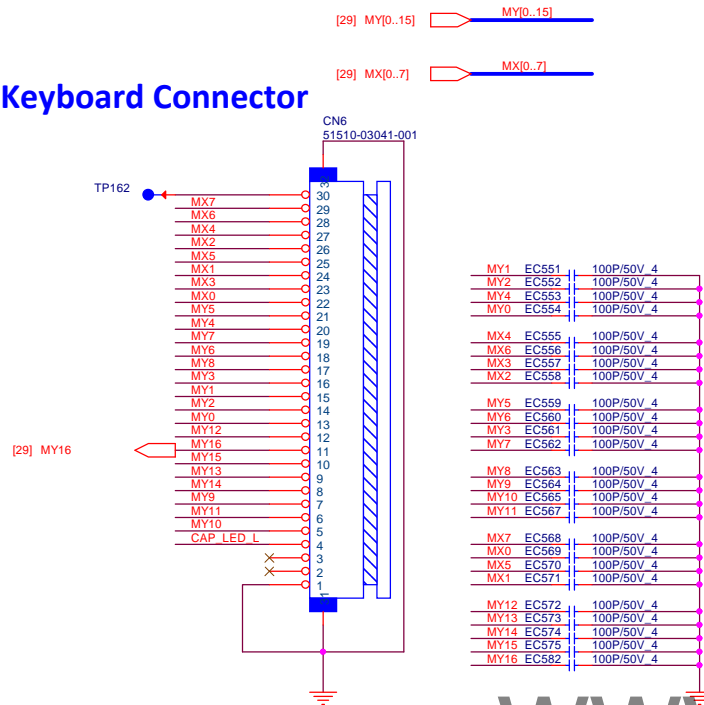
Reserve for EMI and close to HDMI CONN



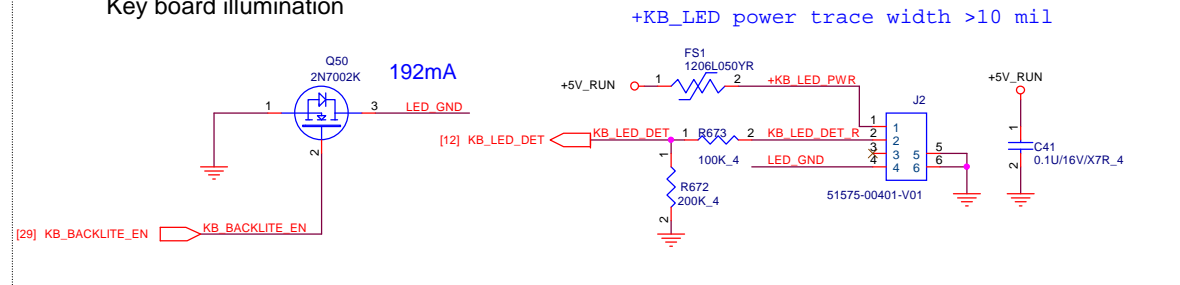
HDMI Conn.



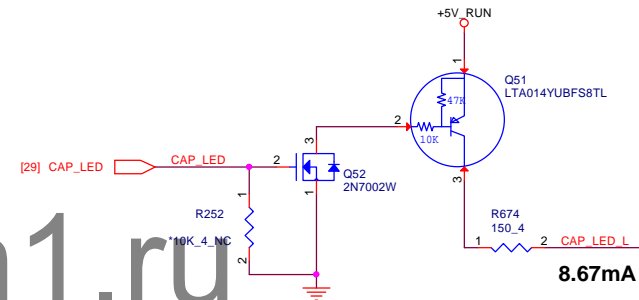
Keyboard Connector



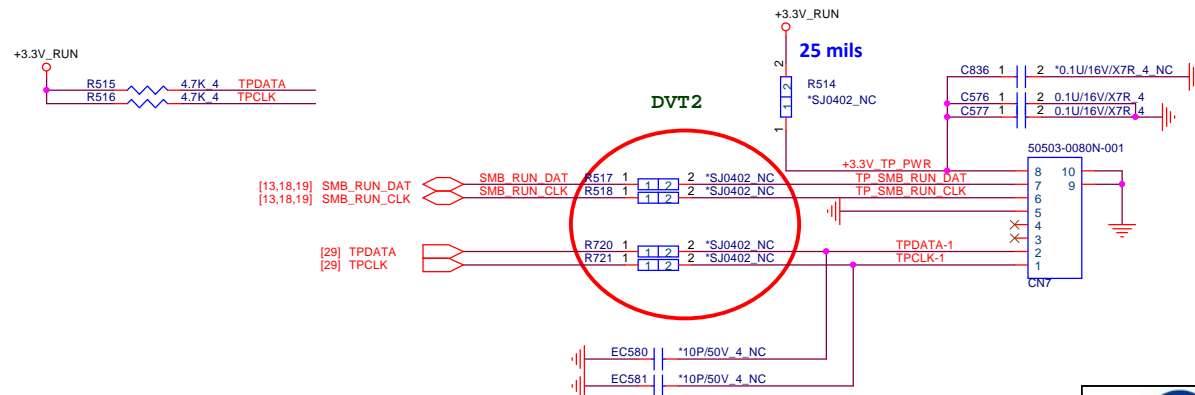
Key board illumination



$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$



Touch Pad Connector

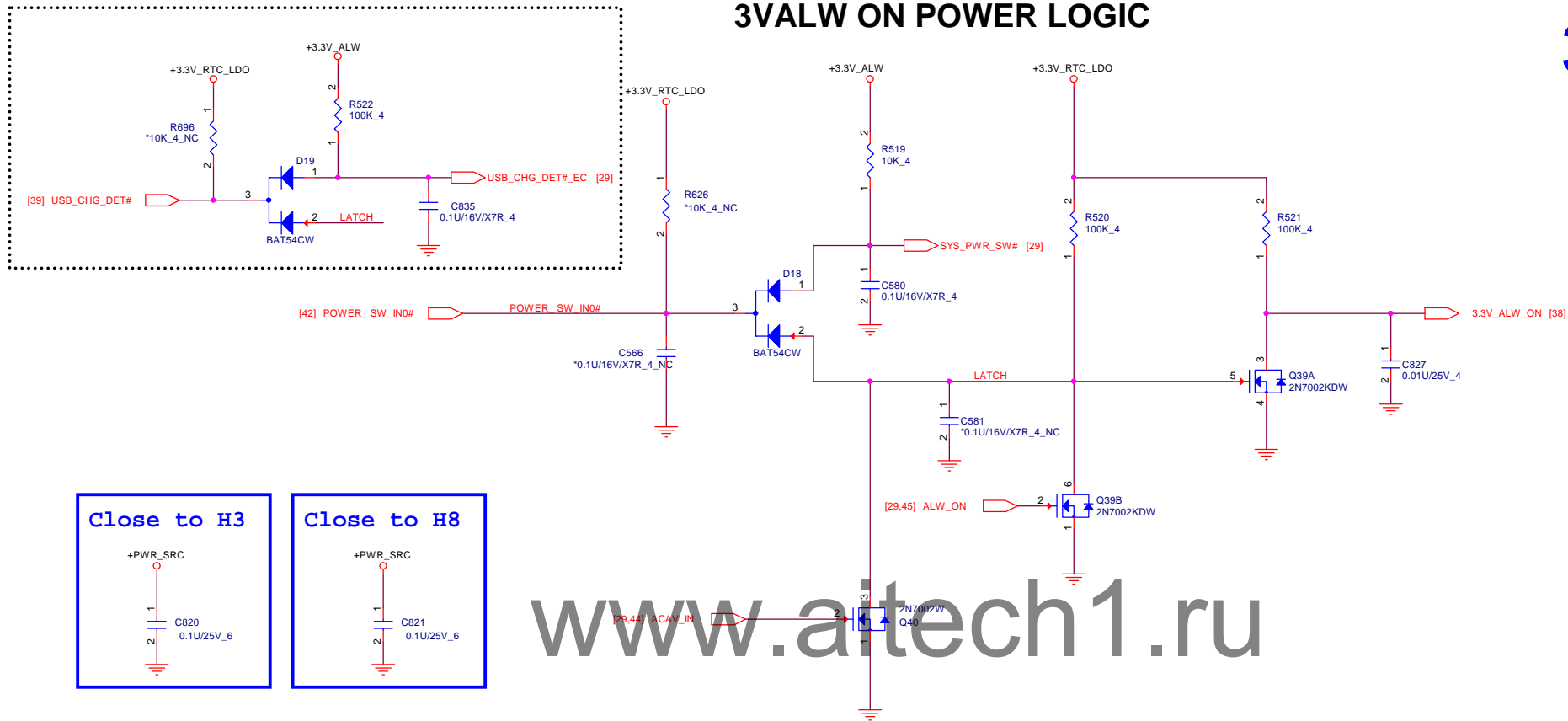


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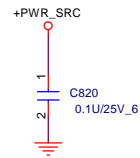
PROJECT : AM7

3VALW ON POWER LOGIC

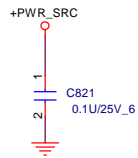
37



Close to H3

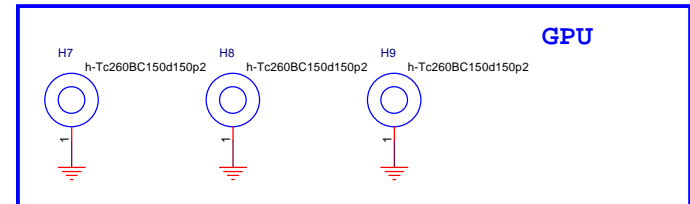
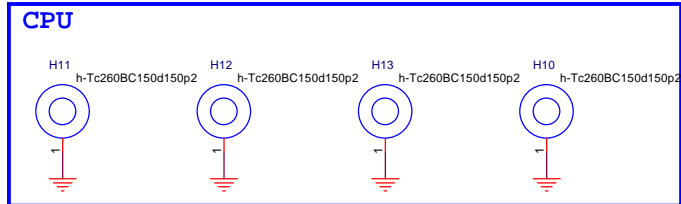
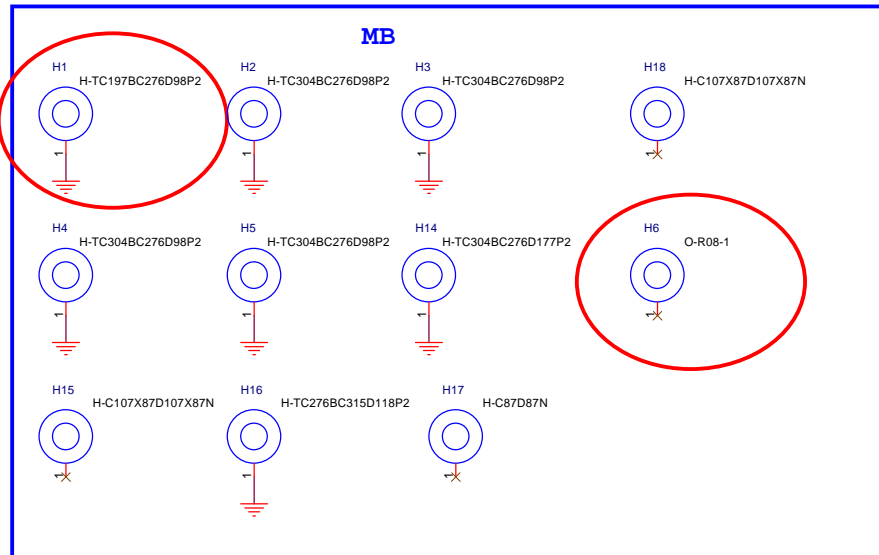


Close to H8



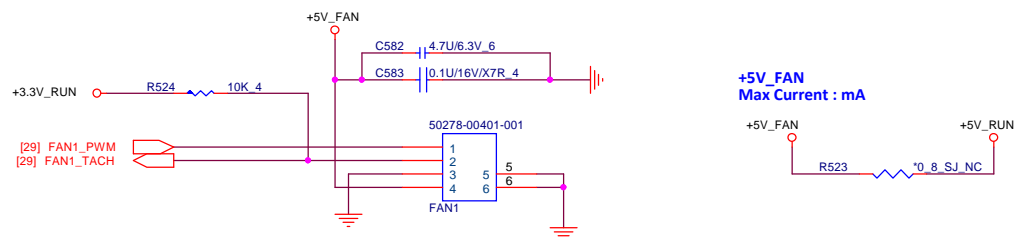
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DVT2



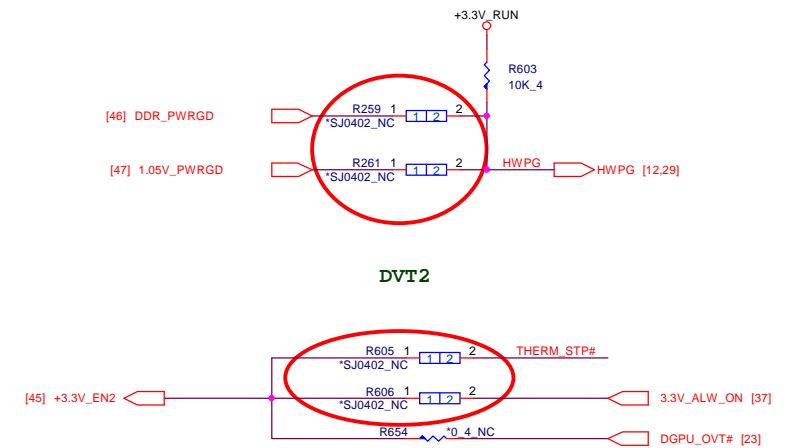
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PROJECT : AM7

FAN CONN

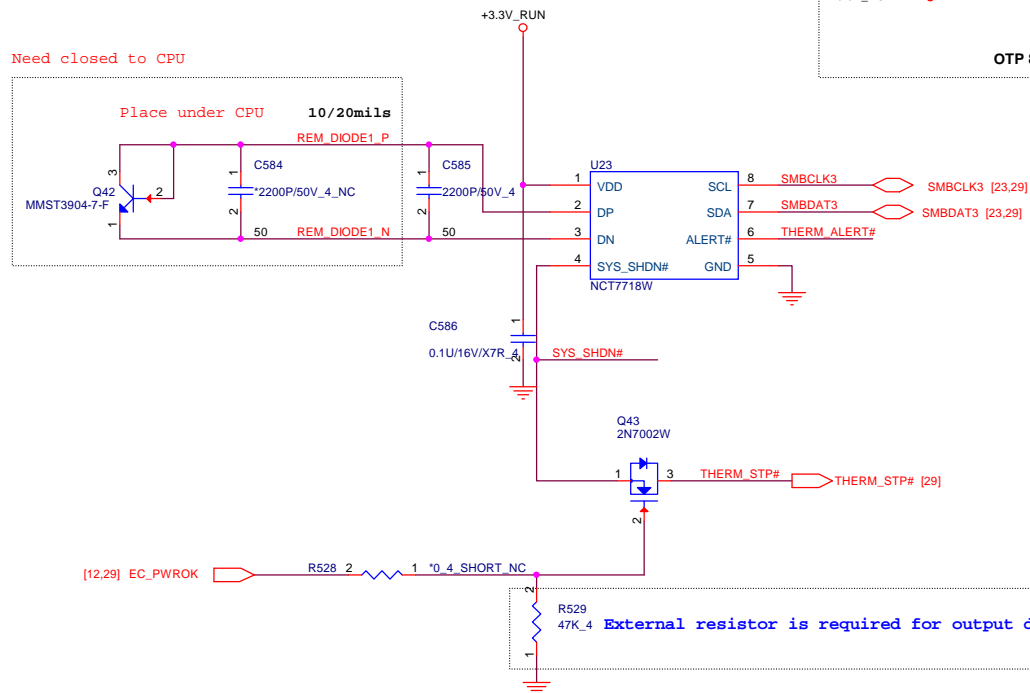


HWPG

38



THERMAL IC



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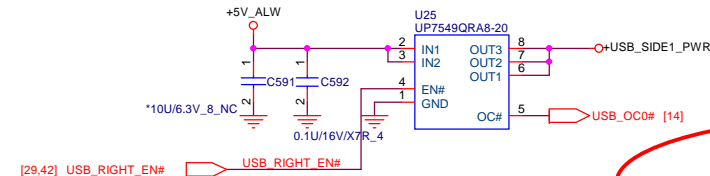
OTP 85 degree C

OTP 85 degree : R526= 18.7K, R527= 2K

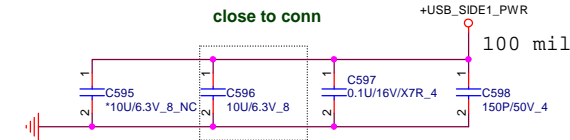
SYS_SHD#					
ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

I continuous 1.5A
OC 2.0A M13 Request

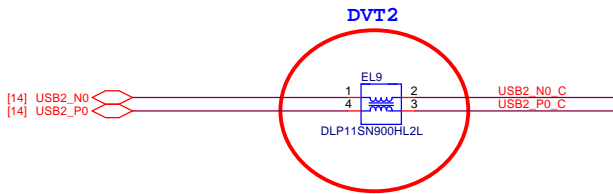
USB3.0/2.0 COMBO X 1



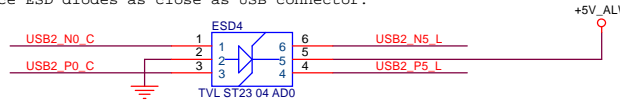
close to conn



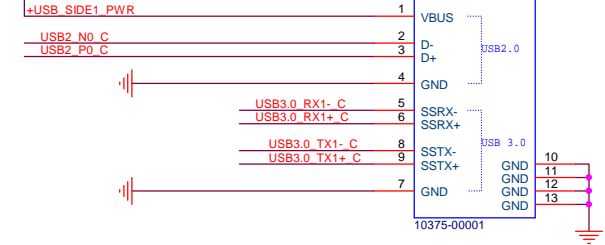
DVT2



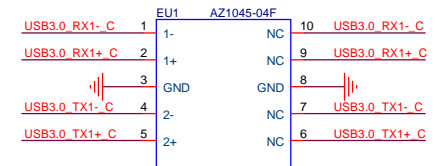
ESD Function
Place ESD diodes as close as USB connector.



+USB_SIDE1_PWR



Need closed to CN8

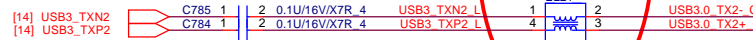


USBP0_BUS_SW_CB0	Mode	Operating at
High	CDP	S0, 1.5 A
Low	DCP, Auto-detect	S3/S4/S5, 2.1/1.5 A

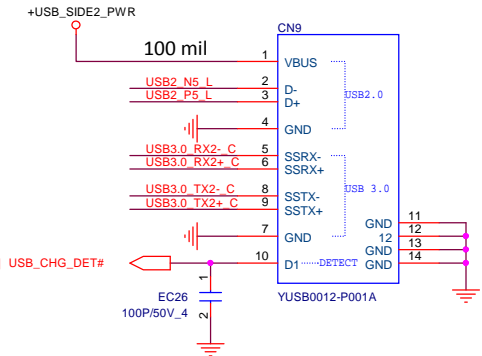
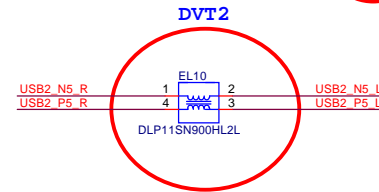
USB Power share



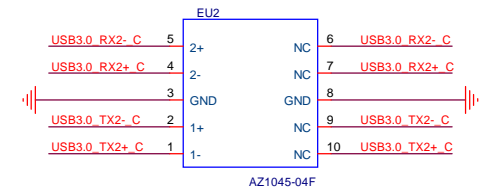
Close to CONN



DVT2



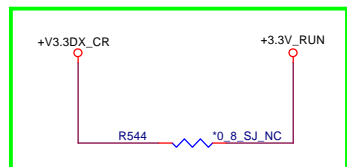
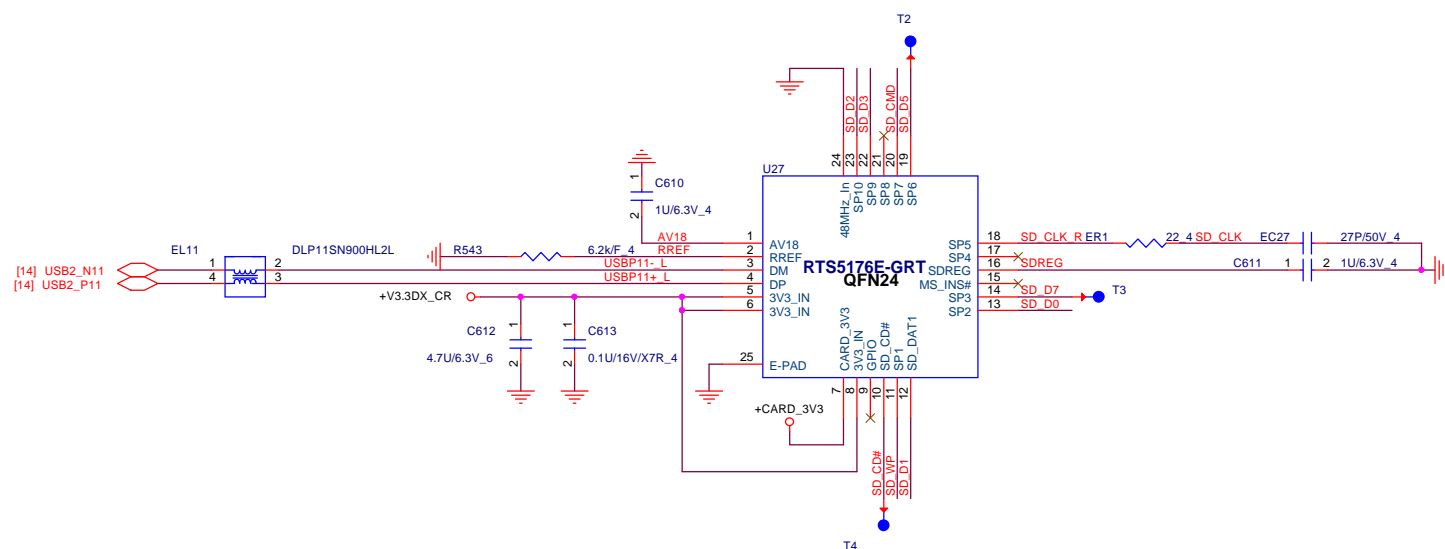
Need closed to CN9



OC limitation	R89	mA
	22.6k ohm	2224
	23.2k ohm	2167

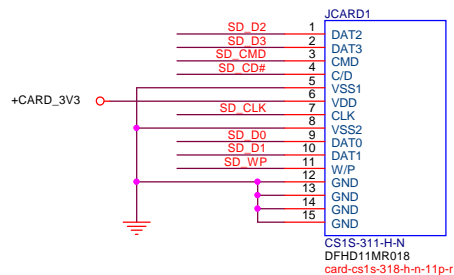
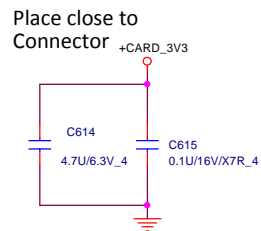


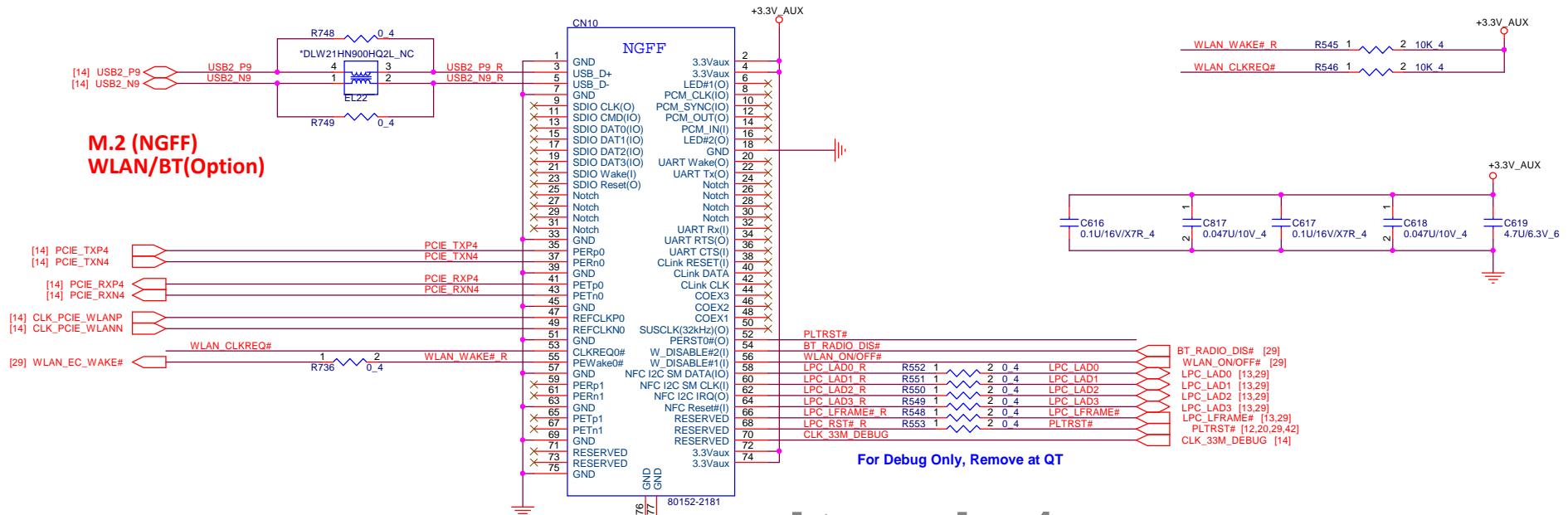
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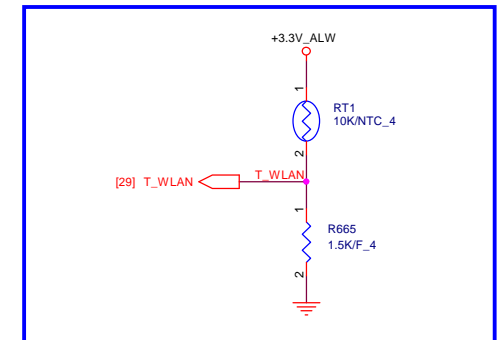
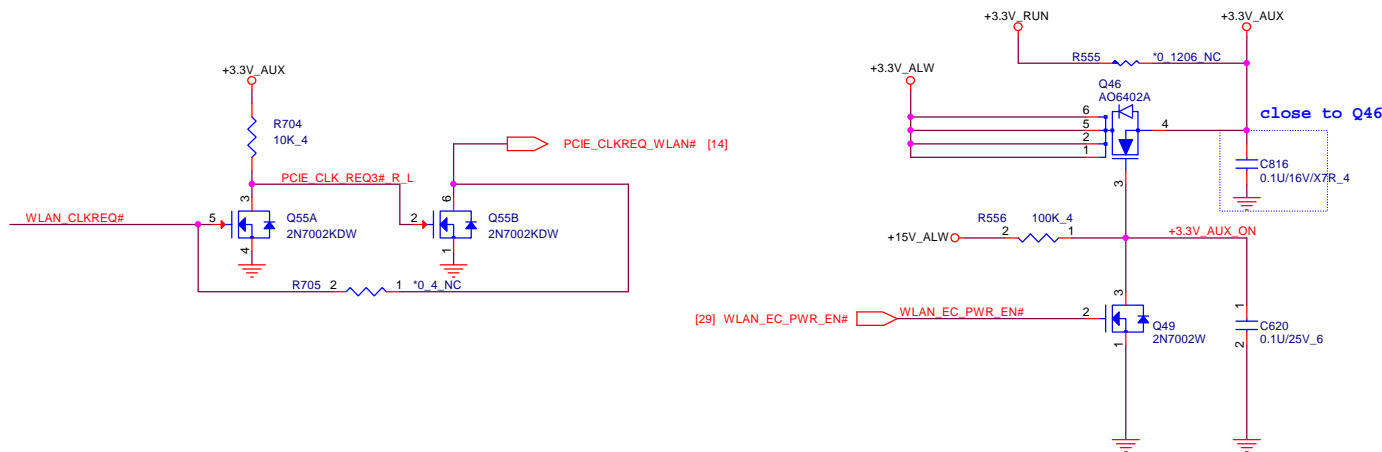
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SD / MMC
CARD READER



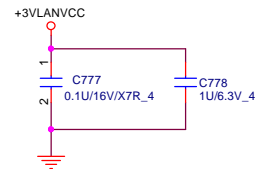
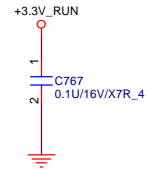
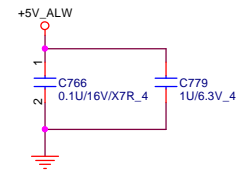
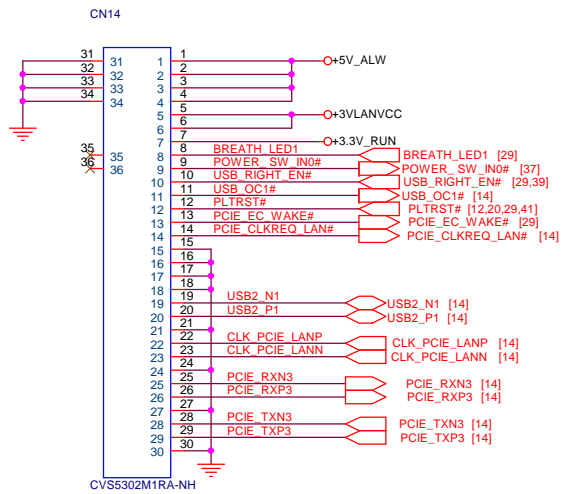


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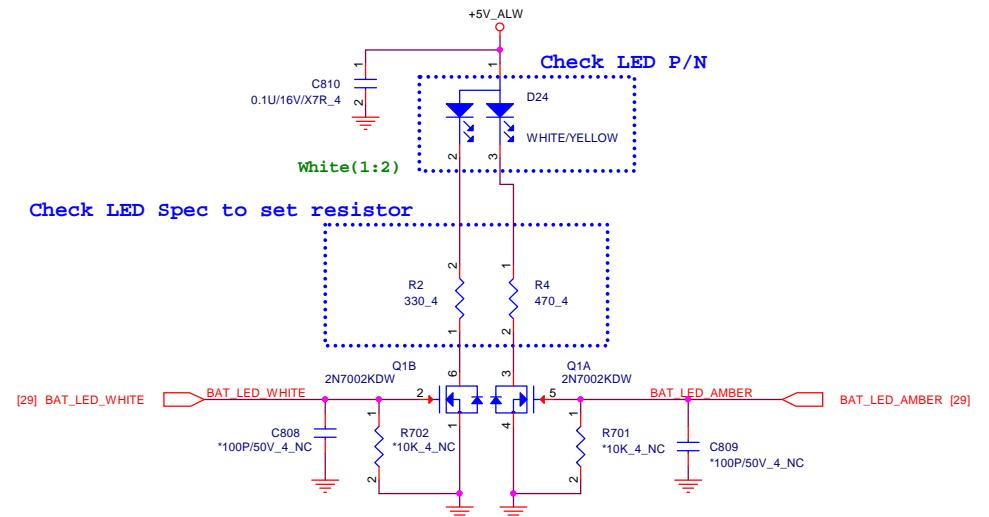


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MB to IO BD Connector

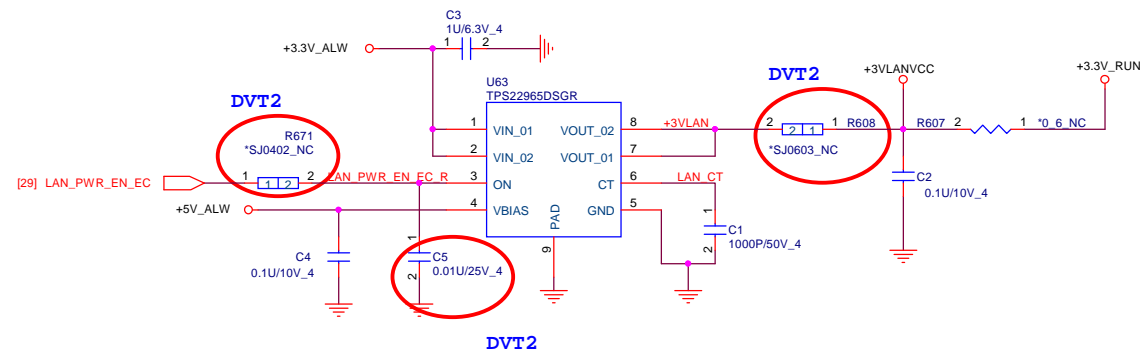


Battery LED



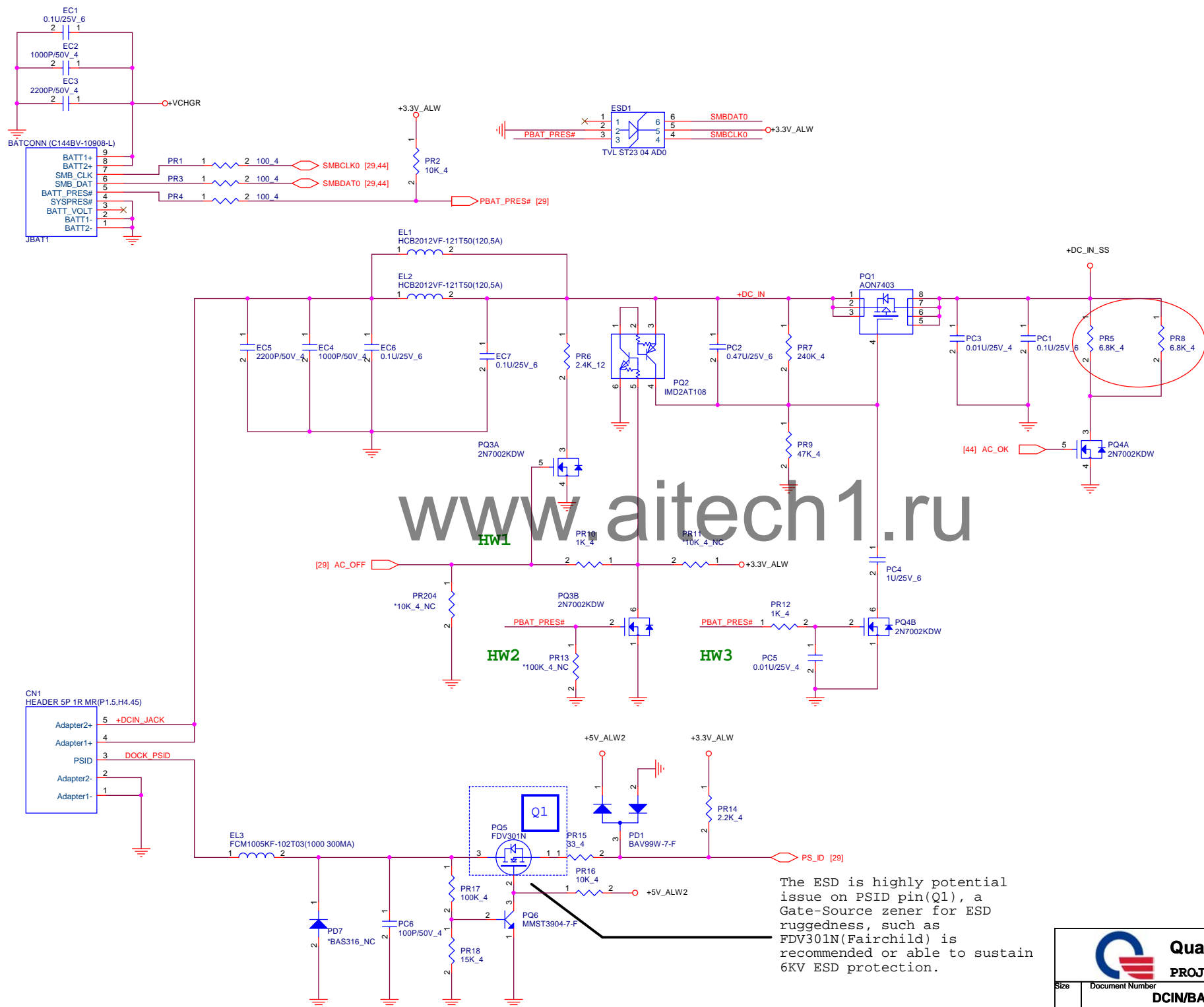
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LAN POWER



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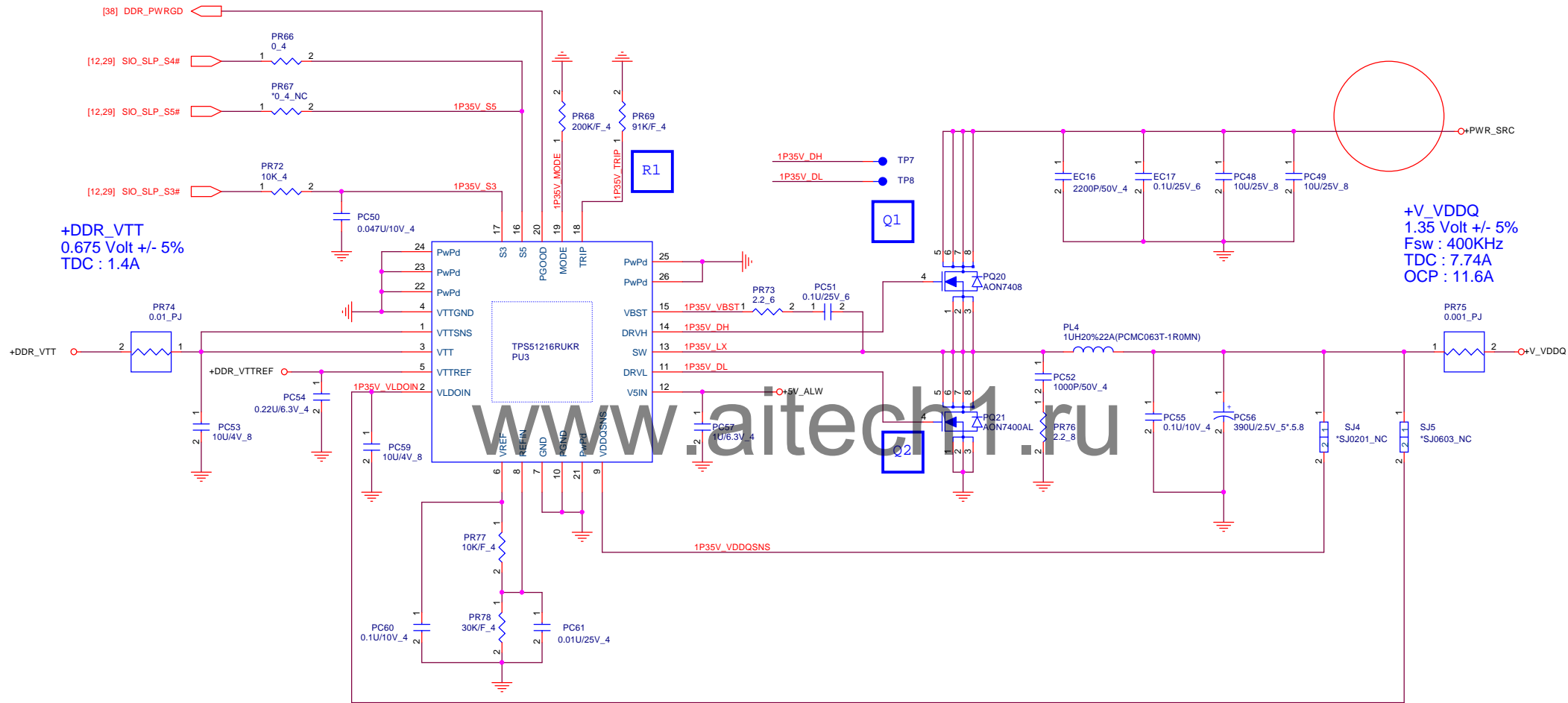


The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.



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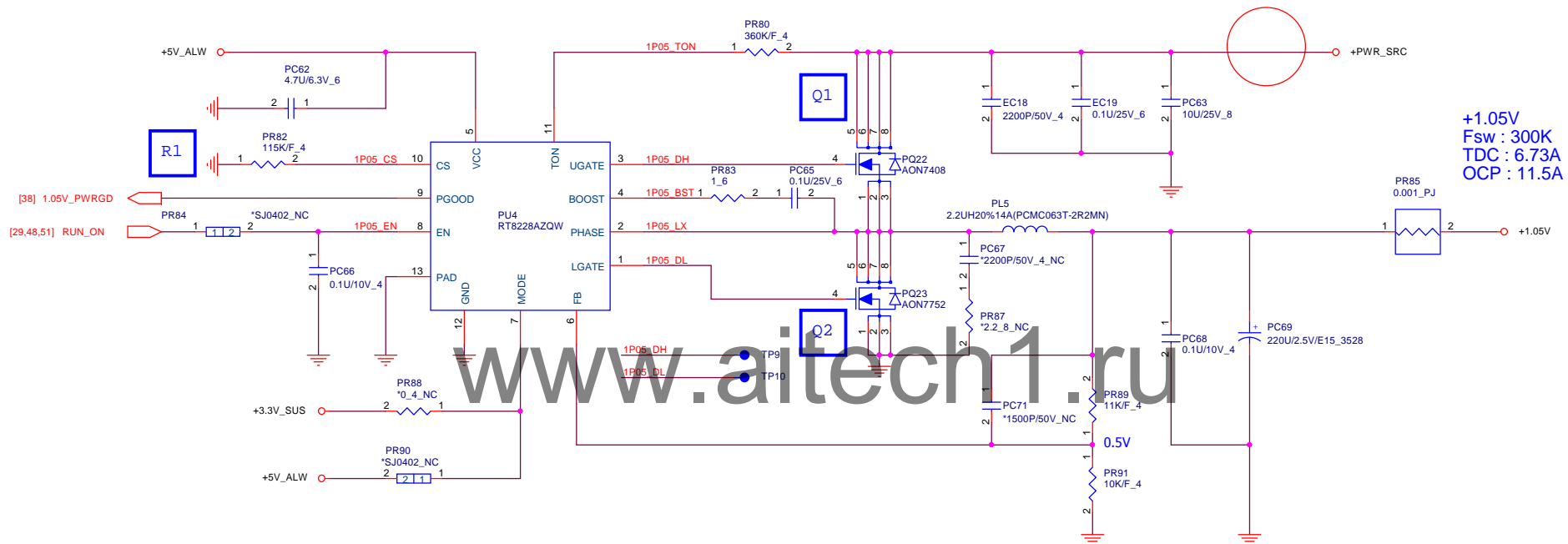
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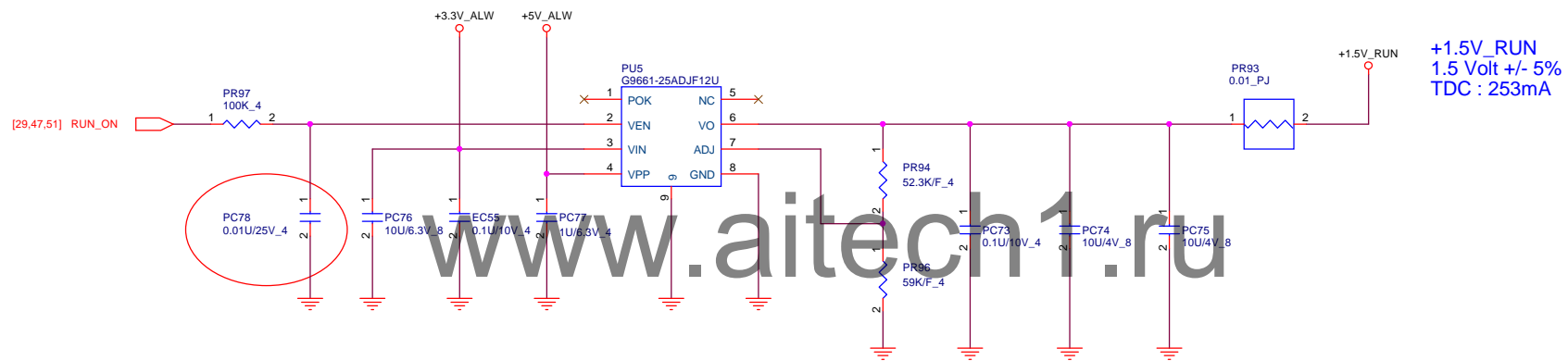
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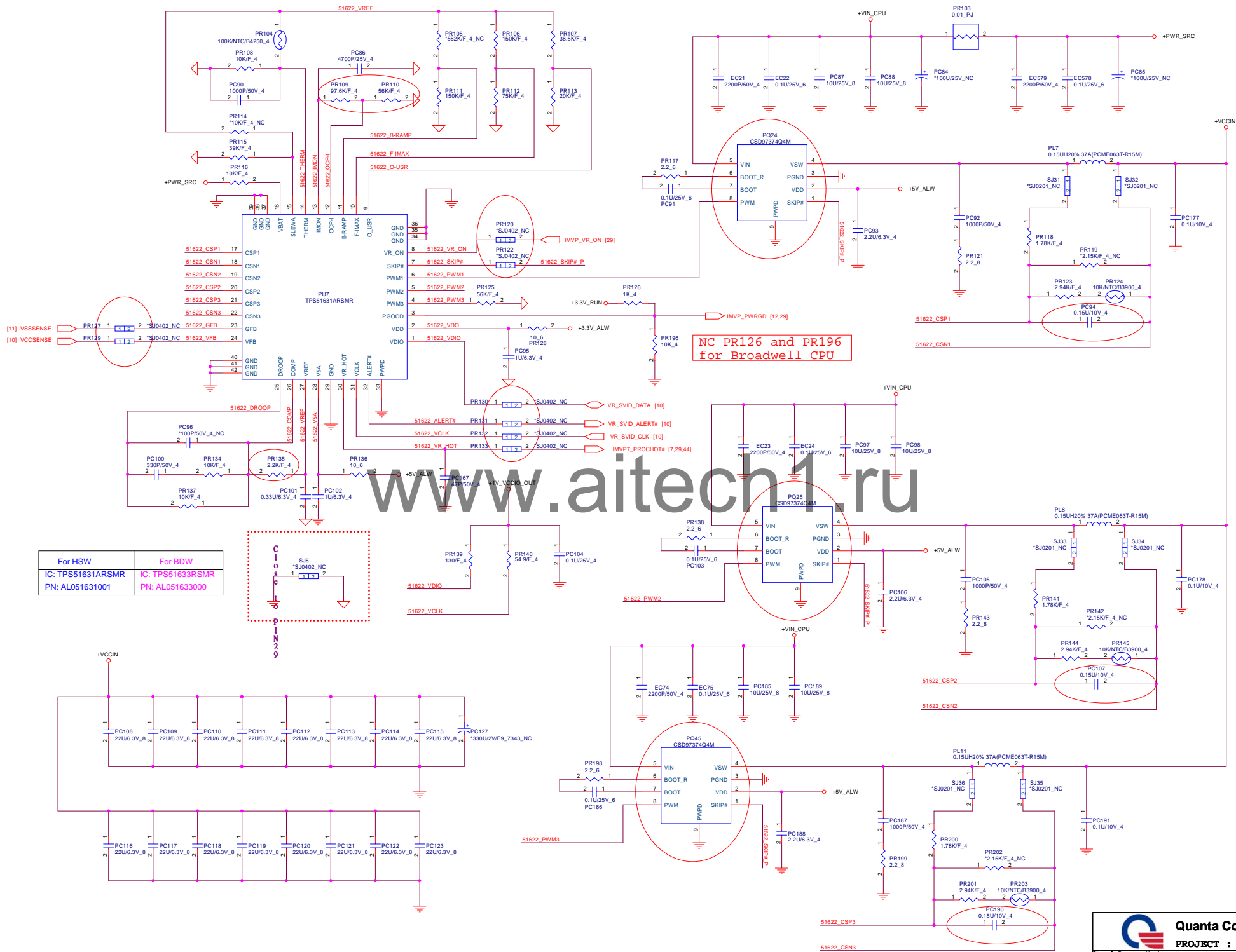
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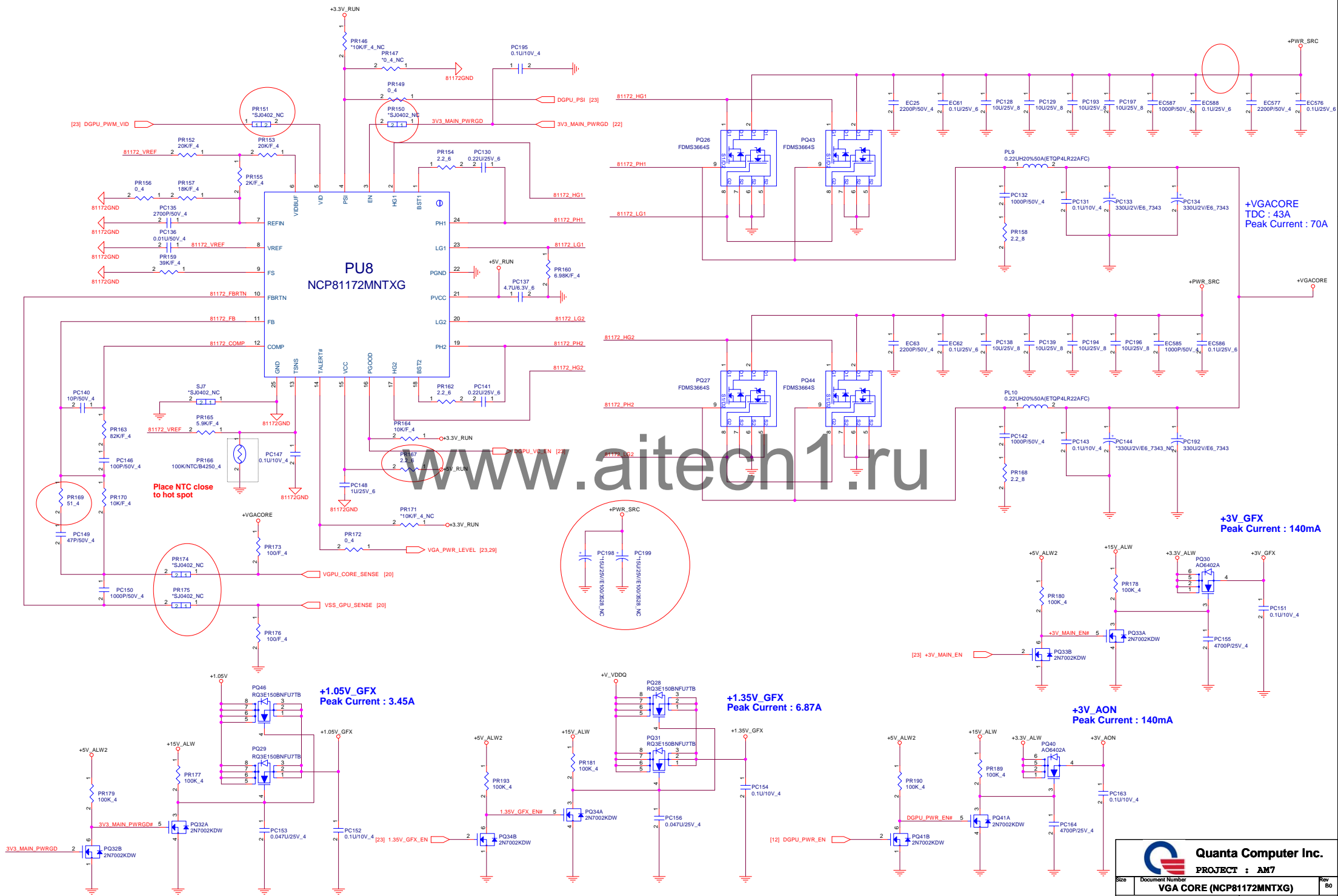


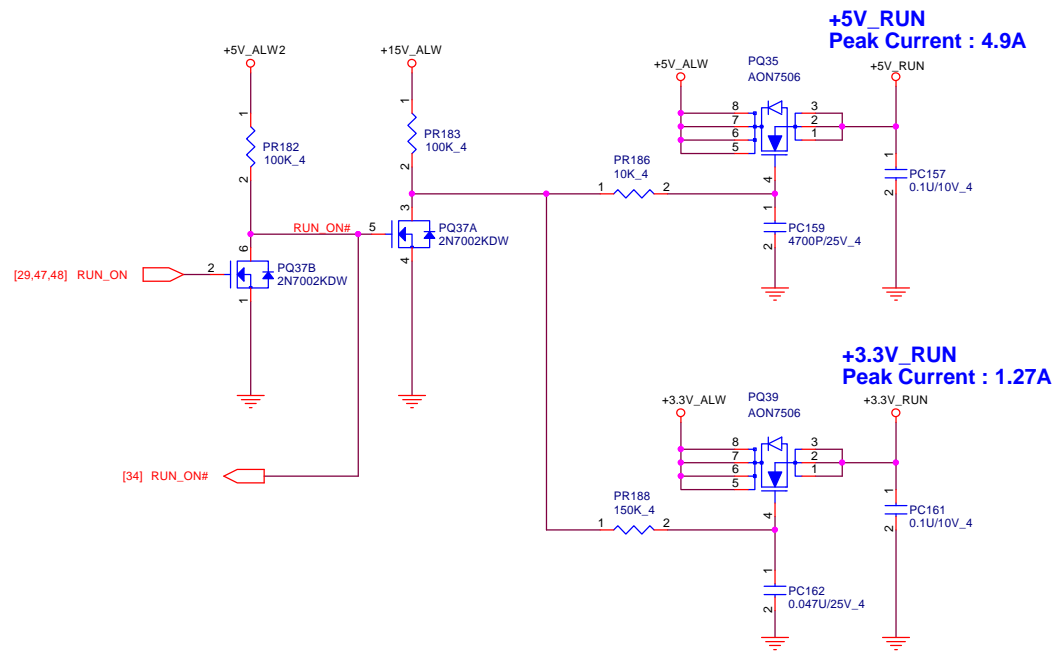
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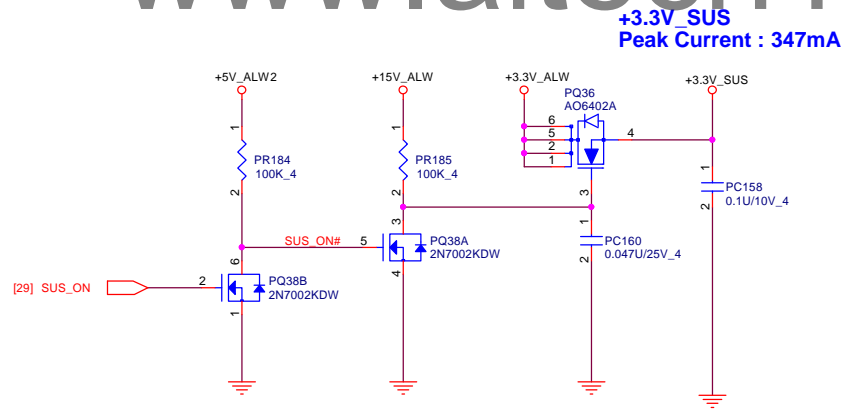
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Date:	Thursday, May 08, 2014	Sheet 48 of 51







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Size	Document Number	Rev
		CO
Date:	Thursday, May 08, 2014	Sheet 51 of 51

SUS_RUN Power Switch